56F8023

Data Sheet

Preliminary Technical Data

56F8000
16-bit Digital Signal Controllers

MC56F8023
Rev. 5
03/2008

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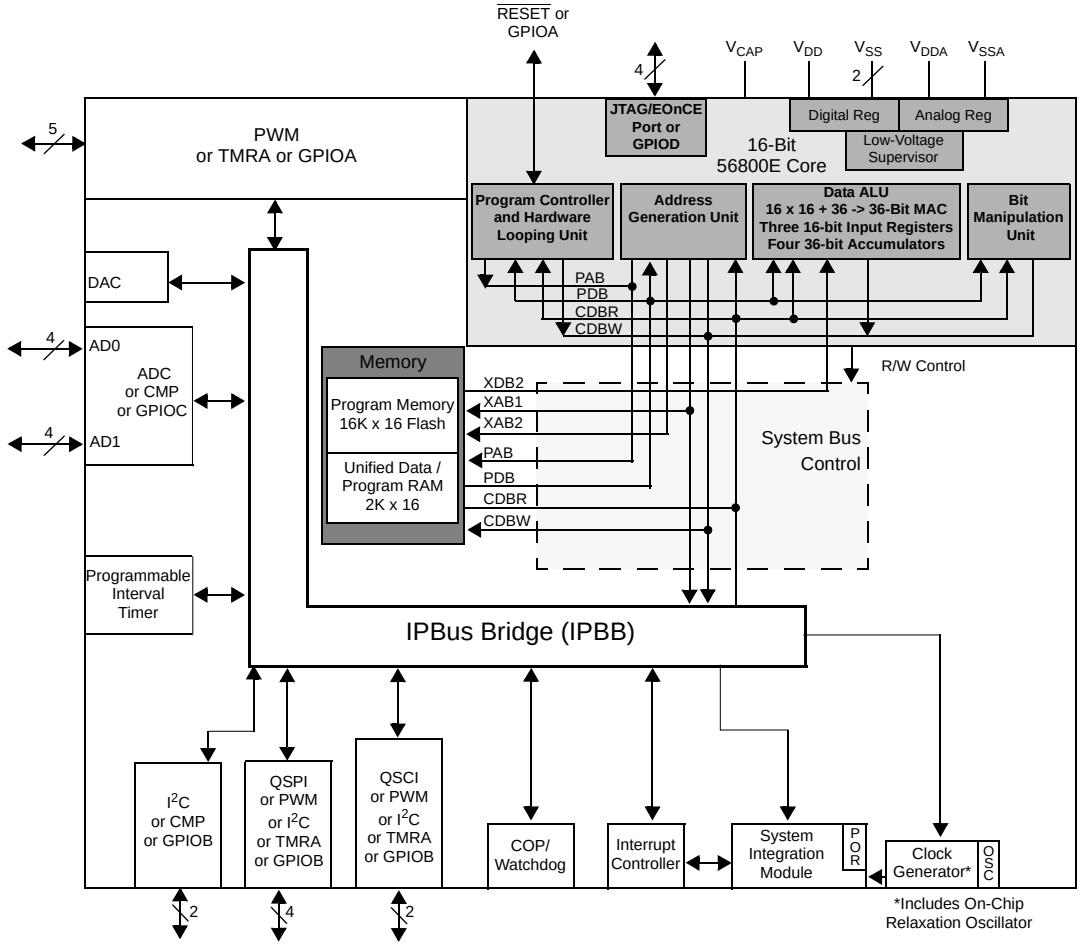
Document Revision History

Version History	Description of Change
Rev. 0	Initial public release.
Rev. 1	• In Table 10-4, added an entry for flash data retention with less than 100 program/erase cycles (minimum 20 years). • In Table 10-6, changed the device clock speed in STOP mode from 8MHz to 4MHz. • In Table 10-12, changed the typical relaxation oscillator output frequency in Standby mode from 400kHz to 200kHz. • Changed input propagation delay values in Table 10-20 as follows: Old values: 1 μs typical, 2 μs maximum New values: 35 ns typical, 45 ns maximum
Rev. 2	In Table 10-19, changed the maximum ADC internal clock frequency from 8 MHz to 5.33 MHz.
Rev. 3	• Added the following note to the description of the TMS signal in Table 2-3: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor. • Corrected pin number labels in Figure 11-1 as follows: Old labels: Pin 1, Pin 12, Pin 23, Pin 34 New labels: Pin 1, Pin 9, Pin 17, Pin 25
Rev. 4	• Changed the ITCN_BASE address In **Table 5-3** (was $00 F060, is $00 F0E0). • Changed the VBA register reset value and updated the footnote in **Section 5.6.8**. • Changed the STANDBY > STOP I_{DD} values in **Table 10-6** as follows: Typical: was 290μA, is 540μA Maximum: was 390μA, is 650μA • Changed the POWERDOWN I_{DD} values in **Table 10-6** as follows: Typical: was 190μA, is 440μA Maximum: was 250μA, is 550μA • Changed footnote 1 in **Table 10-12** (was “Output frequency after application of 8MHz trim value, at 125°C.”, is “Output frequency after application of factory trim”). • Deleted the text “at 125°C” from **Figure 10-5**. • Changed the maximum input offset voltage in **Table 10-20** (was +/- 20 mV, is ±35 mV).
Rev. 5	• Revised **Section 7, Security Features**. • Fixed miscellaneous typos.

Please see http://www.freescale.com for the most current data sheet revision.

56F8023 General Description

- Up to 32 MIPS at 32MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 32KB (16K x 16) Program Flash
- 4KB (2K x 16) Unified Data/Program RAM
- One 6-channel PWM module
- Two 3-channel 12-bit Analog-to-Digital Converters (ADCs)
- Two Internal 12-bit Digital-to-Analog Converters (DACs)
- Two Analog Comparators
- One Programmable Interval Timer (PIT)
- One Queued Serial Communication Interface (QSCI) with LIN slave functionality
- One Queued Serial Peripheral Interfaces (QSPI)
- One 16-bit Quad Timer
- One Inter-Integrated Circuit (I^2C) port
- Computer Operating Properly (COP)/Watchdog
- On-Chip Relaxation Oscillator
- Integrated Power-On Reset (POR) and Low-Voltage Interrupt (LVI) Module
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 26 GPIO lines
- 32-pin LQFP Package



56F8023 Block Diagram

56F8023 Data Sheet Table of Contents

Part 1 Overview

1.1 56F8023 Features

1.1.1 Digital Signal Controller Core

- Efficient 16-bit 56800E family Digital Signal Controller (DSC) engine with dual Harvard architecture
- As many as 32 Million Instructions Per Second (MIPS) at 32MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging

1.1.2 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal Flash
- On-chip memory
  - 32KB of Program Flash
  - 4KB of Unified Data/Program RAM
- EEPROM emulation capability using Flash

1.1.3 Peripheral Circuits for 56F8023

- One multi-function six-output Pulse Width Modulator (PWM) module
  - Up to 96MHz PWM operating clock
  - 15 bits of resolution
  - Center-aligned and edge-aligned PWM signal mode
  - Four programmable fault inputs with programmable digital filter
  - Double-buffered PWM registers
  - Each complementary PWM signal pair allows selection of a PWM supply source from:
    - PWM generator

  - External GPIO
  - Internal timers
  - Analog comparator outputs
  - ADC conversion result which compares with values of ADC high- and low-limit registers to set PWM output
- Two independent 12-bit Analog-to-Digital Converters (ADCs)
  - 2 x 3 channel inputs
  - Supports both simultaneous and sequential conversions
  - ADC conversions can be synchronized by both PWM and timer modules
  - Sampling rate up to 2.67MSPS
  - 16-word result buffer registers
- Two internal 12-bit Digital-to-Analog Converters (DACs)
  - 2 μs settling time when output swing from rail to rail
  - Automatic waveform generation generates square, triangle and sawtooth waveforms with programmable period, update rate, and range
- One 16-bit multi-purpose Quad Timer module (TMR)
  - Up to 96MHz operating clock
  - Eight independent 16-bit counter/timers with cascading capability
  - Each timer has capture and compare capability
  - Up to 12 operating modes
- One Queued Serial Communication Interface (QSCI) with LIN Slave functionality
  - Full-duplex or single-wire operation
  - Two receiver wake-up methods:
    - Idle line
    - Address mark
  - Four-bytes-deep FIFOs are available on both transmitter and receiver
- One Queued Serial Peripheral Interfaces (QSPI)
  - Full-duplex operation
  - Master and slave modes
  - Four-words-deep FIFOs available on both transmitter and receiver
  - Programmable Length Transactions (2 to 16 bits)
- One Inter-Integrated Circuit (I^2C) port
  - Operates up to 400kbps
  - Supports both master and slave operation
  - Supports both 10-bit address mode and broadcasting mode
- One 16-bit Programmable Interval Timer (PIT)
- Two analog Comparators (CMPs)

  - Selectable input source includes external pins, DACs
  - Programmable output polarity
  - Output can drive Timer input, PWM fault input, PWM source, external pin output and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
- Computer Operating Properly (COP)/Watchdog timer capable of selecting different clock sources
- Up to 26 General-Purpose I/O (GPIO) pins with 5V tolerance
- Integrated Power-On Reset and Low-Voltage Interrupt Module
- Phase Lock Loop (PLL) provides a high-speed clock to the core and peripherals
- Clock sources:
  - On-chip relaxation oscillator
  - External clock: Crystal oscillator, ceramic resonator, and external clock source
- JTAG/EOnCE debug programming interface for real-time debugging

1.1.4 Energy Information

- Fabricated in high-density CMOS with 5V tolerance
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 56F8023 Description

The 56F8023 is a member of the 56800E core-based family of Digital Signal Controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F8023 is well-suited for many applications. The 56F8023 includes many peripherals that are especially useful for industrial control, motion control, home appliances, general-purpose inverters, smart sensors, fire and security systems, switched-mode power supply, power management, and medical monitoring applications.

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F8023 supports program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The 56F8023 also offers up to 26 General-Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F8023 Digital Signal Controller includes 32KB of Program Flash and 4KB of Unified Data/Program RAM. Program Flash memory can be independently bulk erased or erased in pages.

Program Flash page erase size is 512 Bytes (256 Words).

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

A full set of programmable peripherals — PWM, ADCs, QSCI, QSPI, I2C, PIT, Quad Timers, DACs, and analog comparators — supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as General Purpose Input/Outputs (GPIOs).

1.4 Architecture Block Diagram

The 56F8023's architecture is shown in **Figures 1-1**, **1-2**, **1-3**, **1-4**, **1-5**, **1-6**, and **1-7**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge and the internal connections between each unit of the 56800E core. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. **Figures 1-3**, **1-4**, **1-5**, **1-6**, and **1-7** detail how the device's I/O pins are muxed. The figures do not show the on-board regulator and power and ground signals. Please see **Part 2, Signal/Connection Descriptions**, for information about which signals are multiplexed with those of other peripherals.

1.4.1 PWM, TMR and ADC Connections

Figure 1-6 shows the over-limit and under-limit connections from the ADC to the PWM and the connections to the PWM from the TMR and GPIO. These signals can control the PWM outputs in a similar manner as the PWM generator. See the **56F802X and 56F803X Peripheral Reference Manual** for additional information.

The PWM_reload_sync output can be connected to the Timer's Channel 3 input and the Timer's Channels 2 and 3 outputs are connected to the ADC sync inputs. Timer Channel 3 output is connected to SYNC0 and Timer Channel 2 is connected to SYNC1. These are controlled by bits in the SIM Control Register; see **Section 6.3.1**.

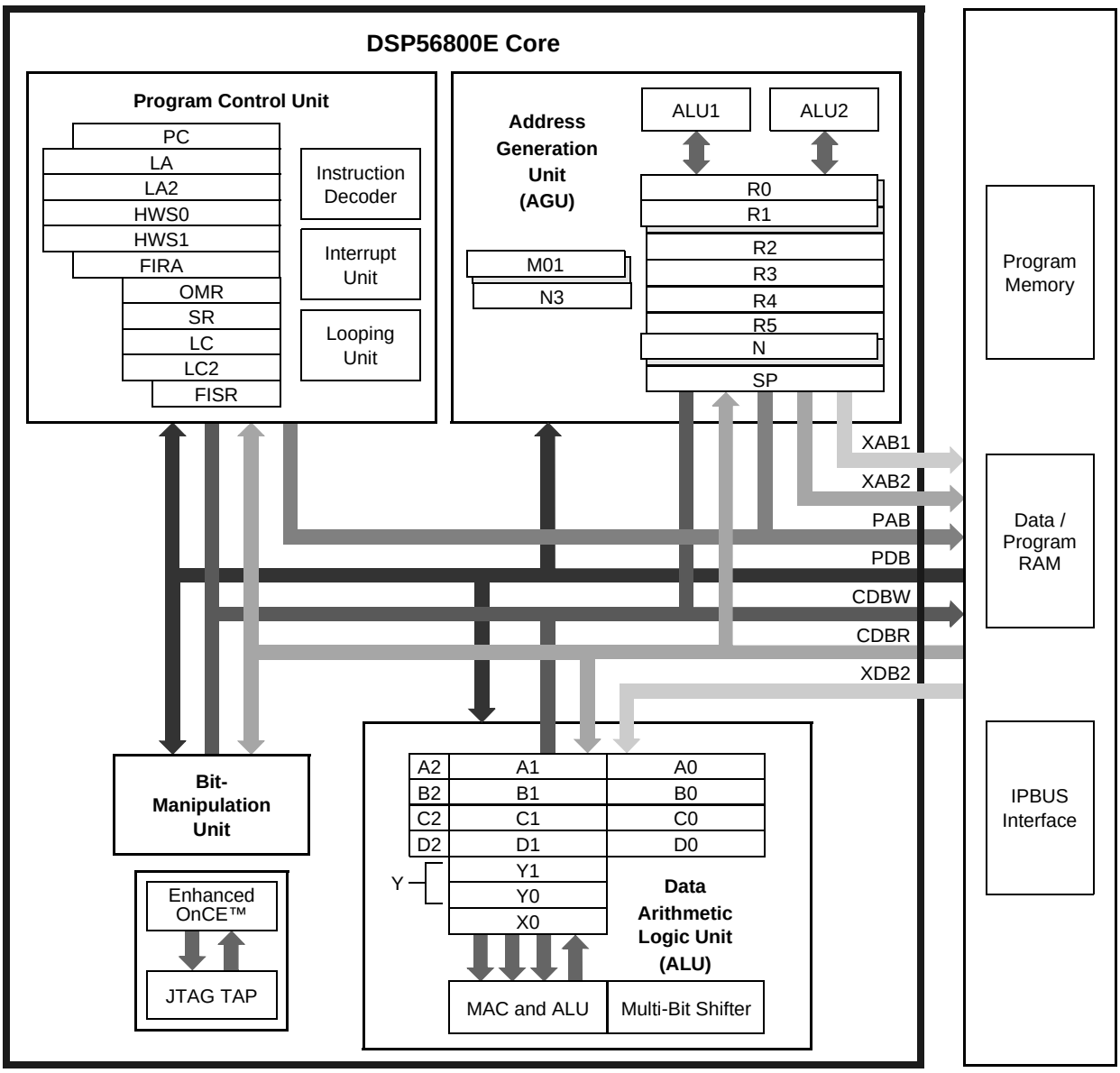


Figure 1-1 56800E Core Block Diagram

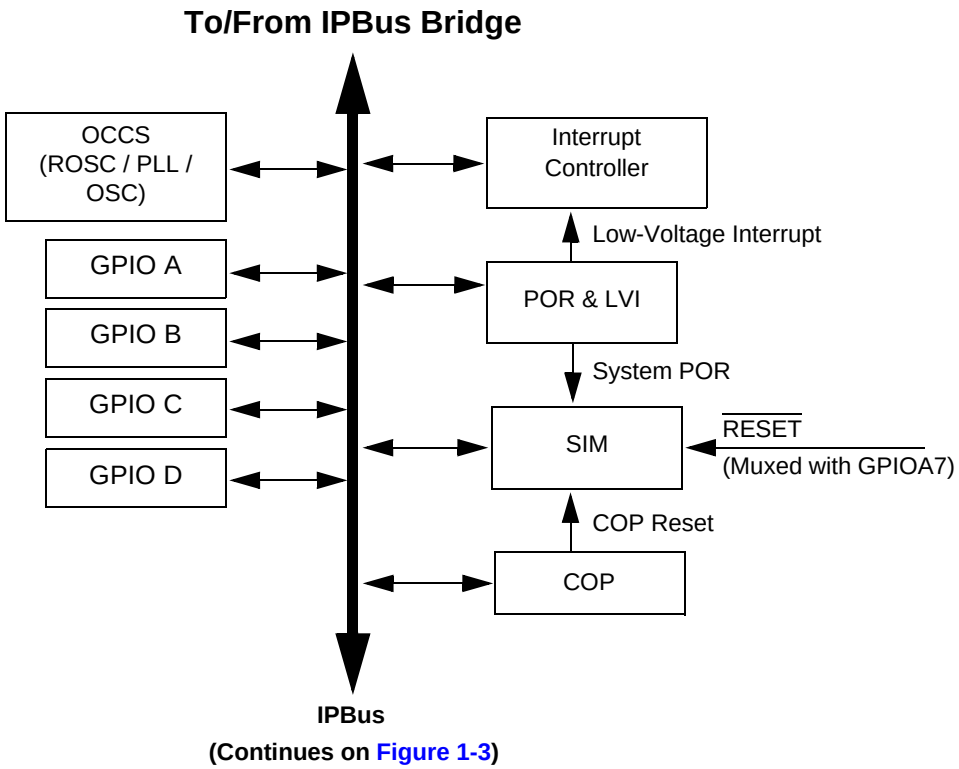


Figure 1-2 Peripheral Subsystem

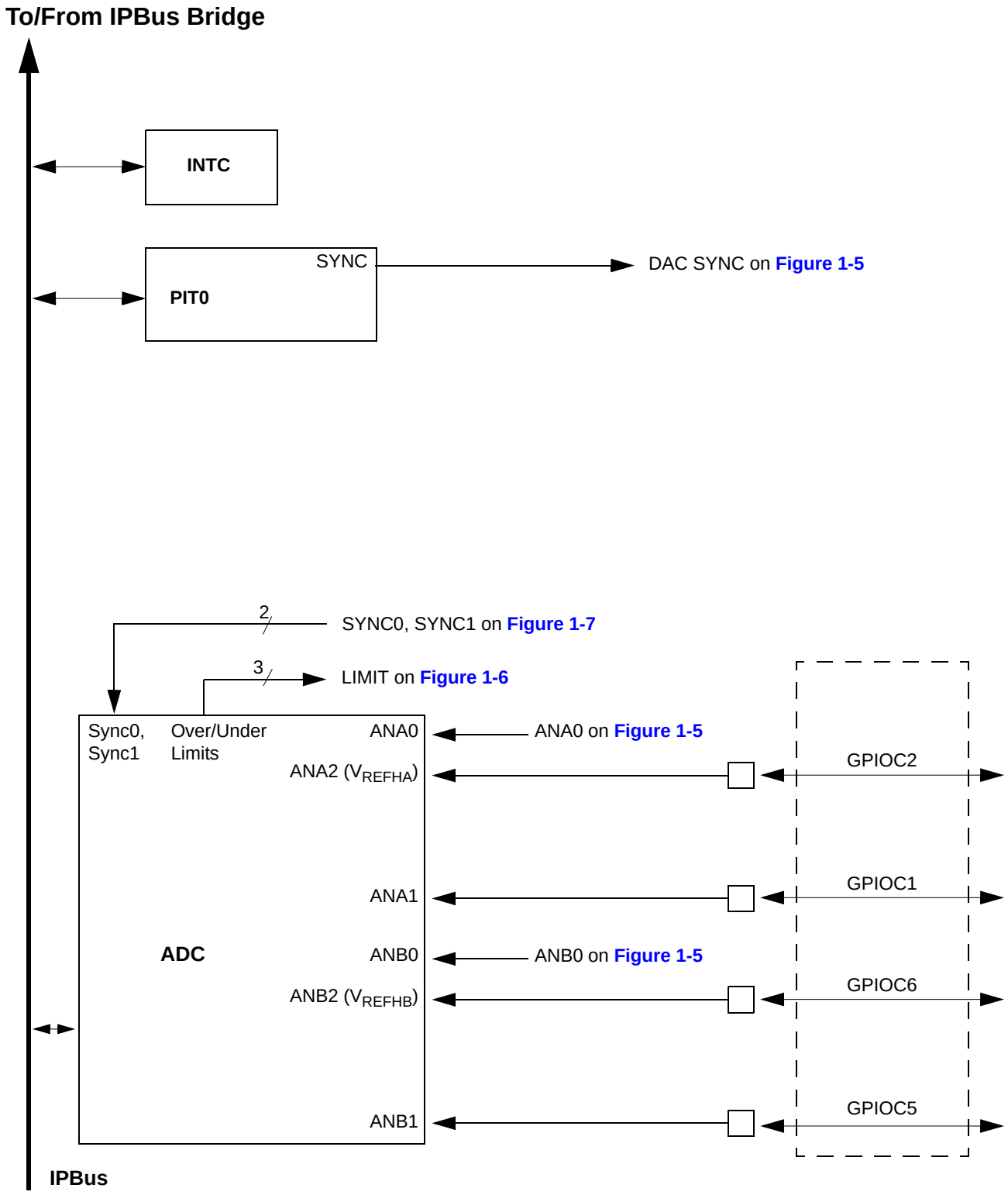


Figure 1-3 56F8023 I/O Pin-Out Muxing (Part 1/5)

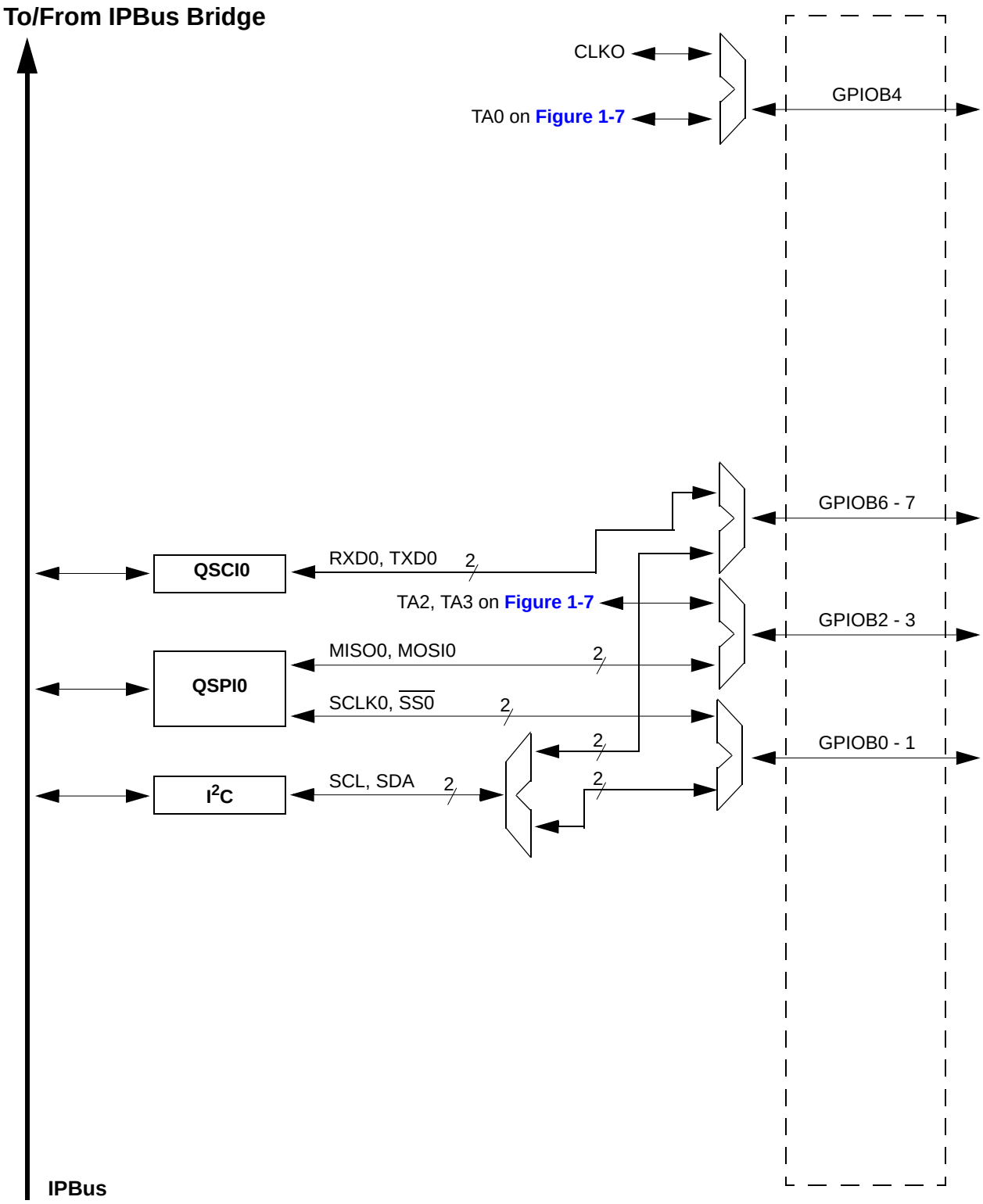


Figure 1-4 56F8023 I/O Pin-Out Muxing (Part 2/5)

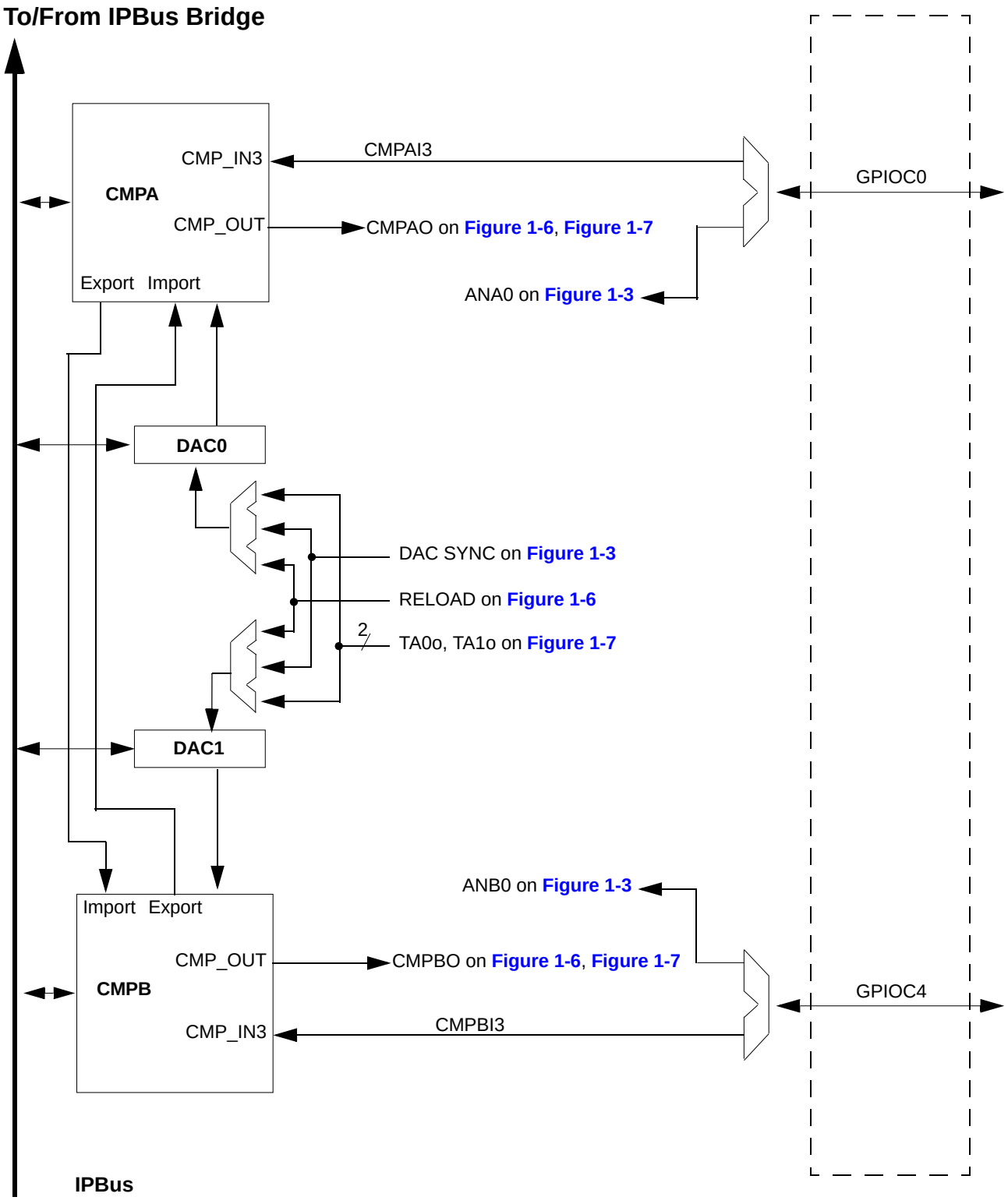


Figure 1-5 56F8023 I/O Pin-Out Muxing (Part 3/5)

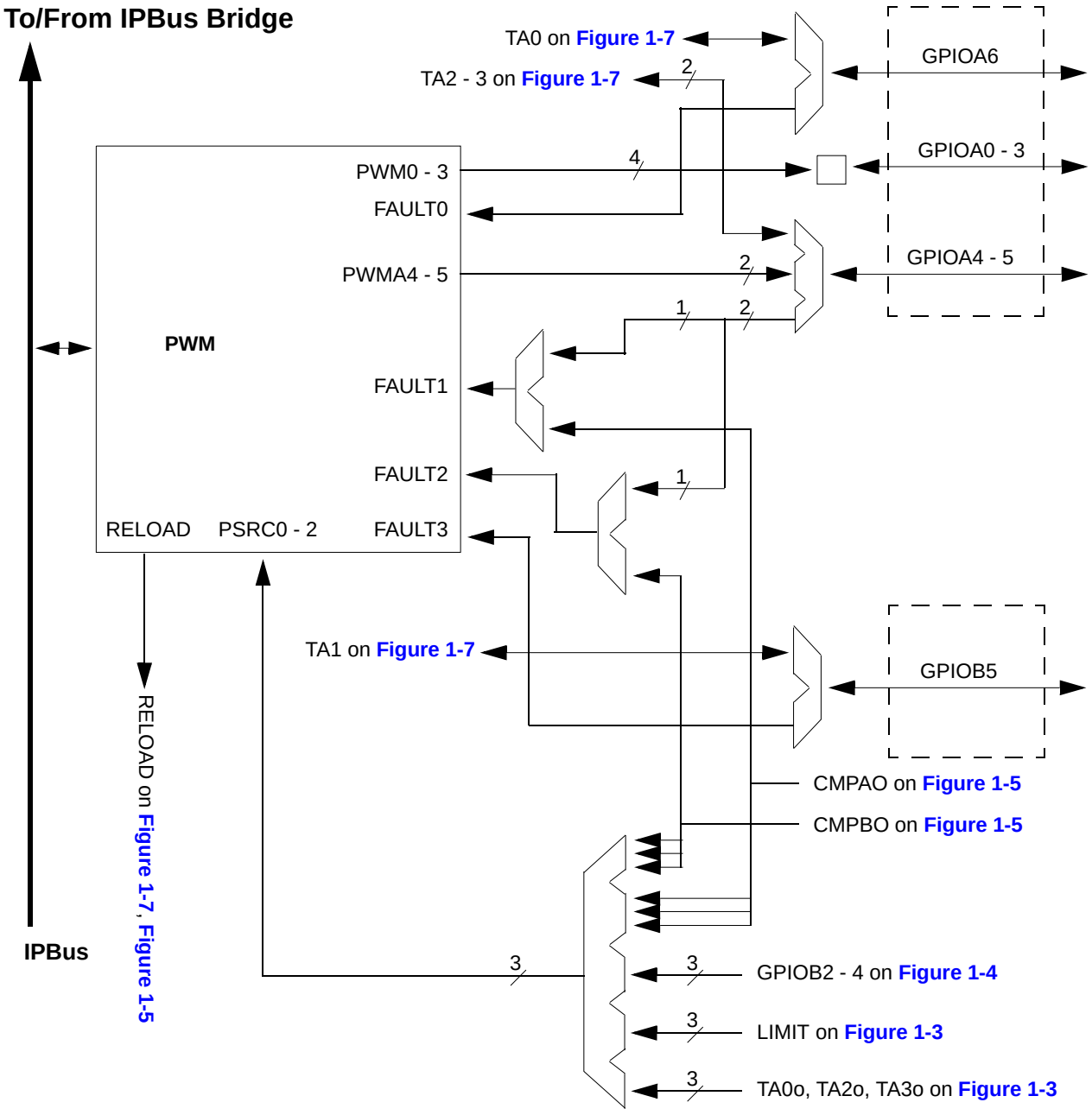


Figure 1-6 56F8023 I/O Pin-Out Muxing (Part 4/5)

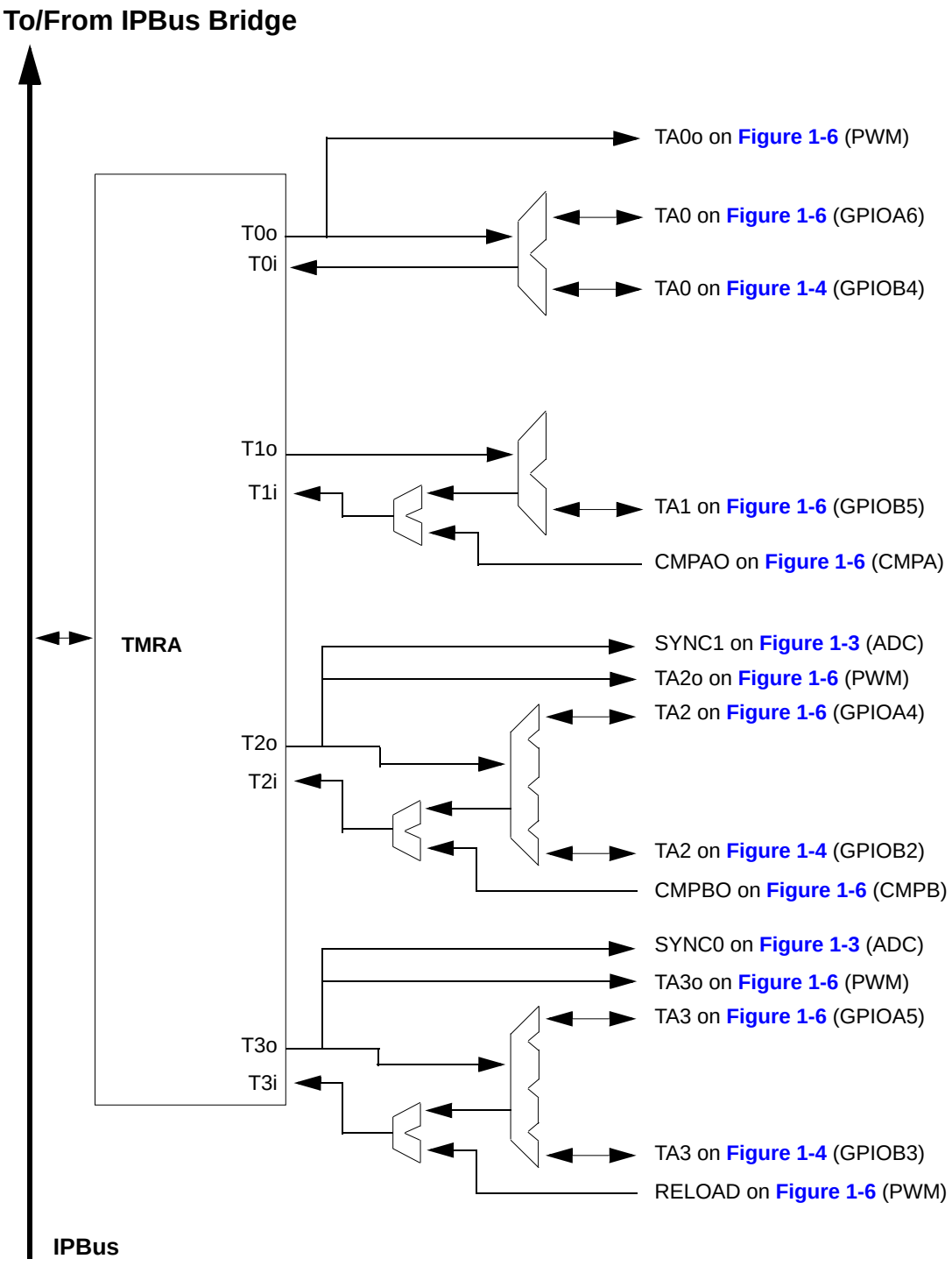


Figure 1-7 56F8023 I/O Pin-Out Muxing (Part 5/5)

1.5 Product Documentation

The documents listed in **Table 1-1** are required for a complete description and proper design with the 56F8023. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at:
http://www.freescale.com

Table 1-1 56F8023 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit Digital Signal Controller core processor, and the instruction set	DSP56800ERM
56F802X and 56F803X Peripheral Reference Manual	Detailed description of peripherals of the 56F802x and 56F803x family of devices	MC56F80xxRM
56F802x and 56F803x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F802x and 56F803x family of devices	56F80xxBLUG
56F8023 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8023
56F8023 Errata	Details any chip issues that might be present	MC56F8023E

1.6 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8023 are organized into functional groups, as detailed in **Table 2-1**. **Table 2-2** summarizes all device pins. In **Table 2-2**, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Power Inputs (V_{DD}, V_{DDA})	2
Ground (V_{SS}, V_{SSA})	3
Supply Capacitors	1
Reset[1]	1
Pulse Width Modulator (PWM) Ports[1]	11
Serial Peripheral Interface (SPI) Ports[1]	4
Timer Module A (TMRA) Ports[1]	4
Analog-to-Digital Converter (ADC) Ports[1]	6
Serial Communications Interface 0 (SCI0) Ports[1]	2
Inter-Integrated Circuit Interface (I^2C) Ports[1]	2
JTAG/Enhanced On-Chip Emulation (EOnCE[1])	4

1. Pins may be shared with other peripherals. See **Table 2-2**.

In **Table 2-2**, peripheral pins in bold identify reset state.

Table 2-2 56F8023 Pins

			Peripherals:										
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**Comp**	**Power & Ground**	**JTAG**	**Misc.**
1	**GPIOB6**	GPIOB6, RXD0, SDA, CLKIN	**B6**	SDA	RXD0								CLKIN
2	**GPIOB1**	GPIOB1, $\overline{SS0}$, SDA	**B1**	SDA		$\overline{SS0}$							
3	**GPIOB7**	GPIOB7, TXD0, SCL	**B7**	SCL	TXD0								
4	**GPIOB5**	GPIOB5, TA1, FAULT3, CLKIN	**B5**					FAULT3	TA1				CLKIN
5	**GPIOC4**	GPIOC4, ANB0 & CMPBI3	**C4**				ANB0			CMPBI3			
6	**GPIOC5**	GPIOC5, ANB1	**C5**				ANB1						
7	**GPIOC6**	GPIOC6, ANB2, V_{REFHB}	**C6**				ANB2 V_{REFHB}						
8	**VDDA**	V_{DDA}									V_{DDA}		
9	**VSSA**	V_{SSA}									V_{SSA}		
10	**GPIOC2**	GPIOC2, ANA2, V_{REFHA}	**C2**				ANA2 V_{REFHA}						
11	**GPIOC1**	GPIOC1, ANA1	**C1**				ANA1						
12	**GPIOC0**	GPIOC0, ANA0 & CMPAI3	**C0**				ANA0			CMPAI3			
13	**VSS**	V_{SS}									V_{SS}		
14	**TCK**	TCK, GPIOD2	D2									**TCK**	
15	**RESET**	$\overline{RESET}$, GPIOA7	A7										**$\overline{RESET}$**
16	**GPIOB3**	GPIOB3, MOSI0, TA3, PSRC1	**B3**			MOSI0		PSRC1	TA3				
17	**GPIOB2**	GPIOB2, MISO0, TA2, PSRC0	**B2**			MISO0		PSRC0	TA2				
18	**GPIOA6**	GPIOA6, FAULT0, TA0	**A6**					FAULT0	TA0				
19	**GPIOB4**	GPIOB4, TA0, CLKO, PSRC2	**B4**					PSRC2	TA0				CLKO
20	**GPIOA5**	GPIOA5, PWM5, TA3, FAULT2	**A5**					PWM5 FAULT2	TA3				
21	**GPIOB0**	GPIOB0, SCLK0, SCL	**B0**	SCL		SCLK0							
22	**GPIOA4**	GPIOA4, PWM4, TA2, FAULT1	**A4**					PWM4 FAULT1	TA2				
23	**GPIOA2**	GPIOA2, PWM2	**A2**					PWM2					
24	**GPIOA3**	GPIOA3, PWM3	**A3**					PWM3					
25	**VCAP**	V_{CAP}									**V_{CAP}**		
26	**VDD**	V_{DD}									**V_{DD}**		
27	**VSS**	V_{SS}									**V_{SS}**		
28	**GPIOA1**	GPIOA1, PWM1	**A1**					PWM1					

Table 2-2 56F8023 Pins (Continued)

			Peripherals:										
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**Comp**	**Power & Ground**	**JTAG**	**Misc.**
29	**GPIOA0**	GPIOA0, PWM0	**A0**					PWM0					
30	**TDI**	TDI, GPIOD0	D0									**TD1**	
31	**TMS**	TMS, GPIOD3	D3									**TMS**	
32	**TDO**	TDO, GPIOD1	D1									**TDO**	

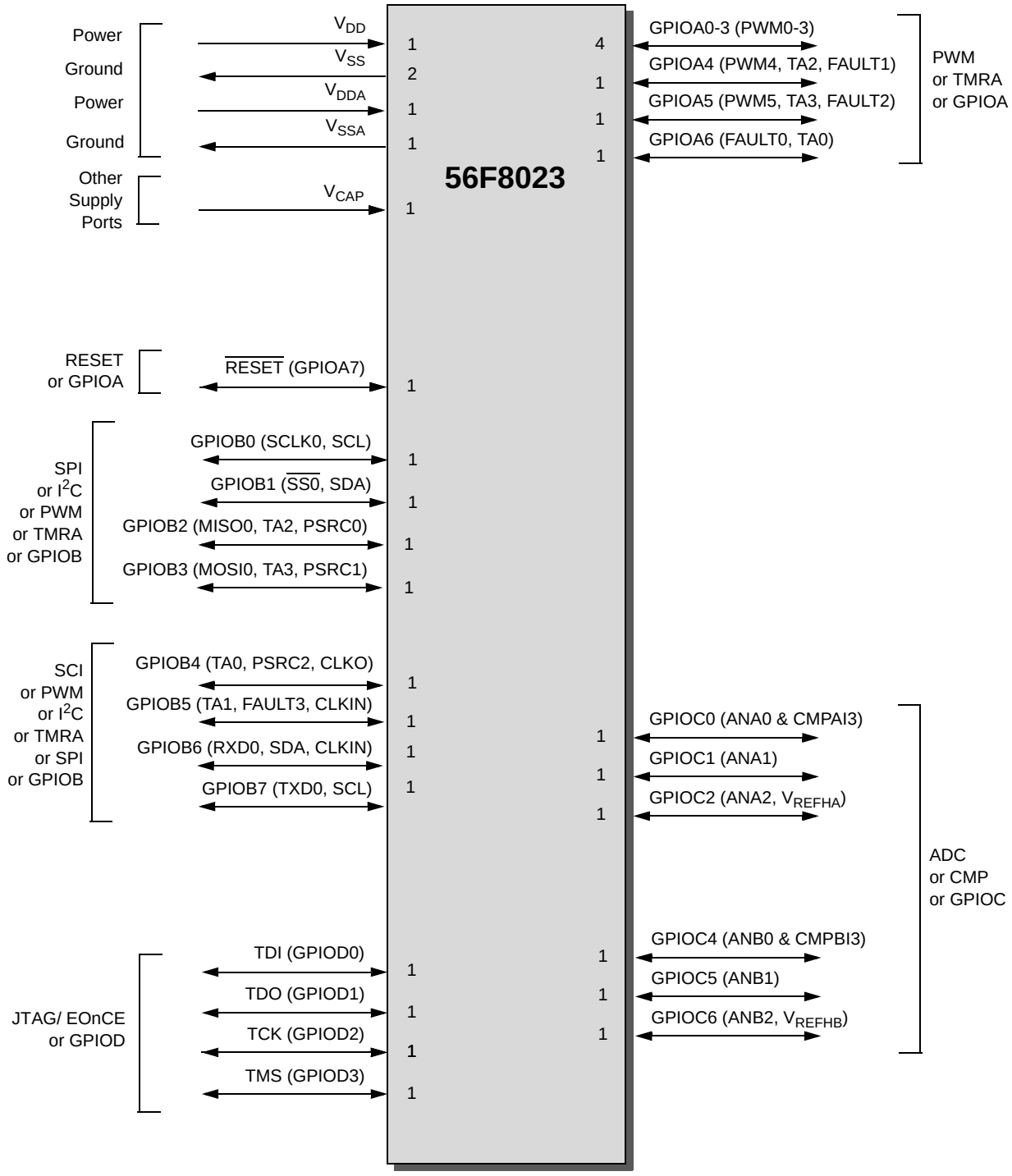


Figure 2-1 56F8023 Signals Identified by Functional Group

2.2 56F8023 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed.

Table 2-3 56F8023 Signal and Package Information for the 32-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
V_{DD}	26	Supply	Supply	**I/O Power** — This pin supplies 3.3V power to the chip I/O interface.
V_{SS}	13	Supply	Supply	**V_{SS}** — These pins provide ground for chip logic and I/O drivers.
V_{SS}	27			
V_{DDA}	8	Supply	Supply	**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SSA}	9	Supply	Supply	**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
V_{CAP}	25	Supply	Supply	**V_{CAP}** — Connect this pin to a 4.7μF or greater bypass capacitor in order to bypass the core voltage regulator, required for proper chip operation. See **Section 10.2.1**.
$\overline{\text{RESET}}$ **(GPIOA7)**	15	Input Input/Open Drain Output	Input, internal pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the chip is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks. **Port A GPIO** — This GPIO pin can be individually programmed as an input or open drain output pin. Note that $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can only be reset via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOA0 **(PWM0)**	29	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM0** — This is one of the six PWM output pins. After reset, the default state is GPIOA0.

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Table 2-3 56F8023 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA1 **(PWM1)**	28	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM1** — This is one of the six PWM output pins. After reset, the default state is GPIOA1.
GPIOA2 **(PWM2)**	23	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM2** — This is one of the six PWM output pins. After reset, the default state is GPIOA2.
GPIOA3 **(PWM3)**	24	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM3** — This is one of the six PWM output pins. After reset, the default state is GPIOA3.
GPIOA4 **(PWM4)** **(TA2[1])** **(FAULT1[2])**	22	Input/ Output Output Input/ Output Input	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM4** — This is one of the six PWM output pins. **TA2** — Timer A, Channel 2 **Fault1** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. After reset, the default state is GPIOA4. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.

[1]The TA2 signal is also brought out on the GPIOB2-3 pin.
[2]The Fault1 signal is also brought out on the GPIOB4 pin.

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Table 2-3 56F8023 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA5	20	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(PWM5)		Output		**PWM5** — This is one of the six PWM output pins.
(TA3[3])		Input/ Output		**TA3** — Timer A, Channel 3
(FAULT2[4])		Input		**Fault2** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. After reset, the default state is GPIOA5. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[3]The TA3 signal is also brought out on the GPIOB2-3 pin. [4]The Fault2 signal is also brought out on the GPIOB4 pin.				
GPIOA6	18	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(FAULT0)		Input		**Fault0** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TA0[5])				**TA0** — Timer A, Channel 0. After reset, the default state is GPIOA6. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[5]The TA0 signal is also brought out on the GPIOB4 pin.				

Return to Table 2-2

Table 2-3 56F8023 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB0	21	Input/ Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SCLK0)		Input/ Output		**QSPI0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(SCL[6])		Input/ Output		**Serial Clock** — This pin serves as the I^2C serial clock. After reset, the default state is GPIOB0. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[6]The SCL signal is also brought out on the GPIOB7 pin.				
GPIOB1	2	Input/ Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
($\overline{SS0}$)		Input/ Output		**QSPI0 Slave Select** — $\overline{SS}$ is used in slave mode to indicate to the QSPI0 module that the current transfer is to be received.
(SDA[7])		Input		**Serial Data** — This pin serves as the I^2C serial data line. After reset, the default state is GPIOB1. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[7]The SDA signal is also brought out on the GPIOB6 pin.				

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Table 2-3 56F8023 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB2	17	Input/ Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(MISO0)		Input/ Output		**QSPI0 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data.
(TA2[8])		Input/ Output		**TA2** — Timer A, Channel 2
(PSRC0)		Input		**PSRC0** — External PWM signal source input for the complementary PWM4/PWM5 pair. After reset, the default state is GPIOB2. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[8]The TA2 signal is also brought out on the GPIOA4 pin.				
GPIOB3	16	Input/ Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(MOSI0)		Input/ Output		**QSPI0 Master Out/Slave In**— This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data.
(TA3[9])		Input/ Output		**TA3** — Timer A, Channel 3
(PSRC1)		Input		**PSRC1** — External PWM signal source input for the complementary PWM2/PWM3 pair. After reset, the default state is GPIOB3. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[9]The TA3 signal is also brought out on the GPIOA5 pin.				

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Table 2-3 56F8023 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB4 **(TA0[10])** **(PSRC2)** **(CLKO)**	19	Input/ Output Input/ Output Input Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **TA0** — Timer A, Channel 0 **PSRC2** — External PWM signal source input for the complementary PWM0/PWM1 pair. **Clock Output** — This is a buffered clock output; the clock source is selected by Clockout Select (CLKOSEL) bits in the Clock Output Select Register (CLKOUT). See **Section 6.3.7**. After reset, the default state is GPIOB4. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[10]The TA0 signal is also brought out on the GPIOB4 and GPIOA6 pins.				
GPIOB5 **(TA1)** **(FAULT3)** **(CLKIN)**	4	Input/ Output Input/ Output Input Input	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **TA1** — Timer A, Channel 1 **FAULT3** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. **External Clock Input**— This pin serves as an external clock input. After reset, the default state is GPIOB5. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.

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Table 2-3 56F8023 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB6	1	Input/ Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(RXD0)		Input		**Receive Data 0** — QSCI0 receive data input.
(SDA[11])		Input/ Output		**Serial Data** — This pin serves as the I^2C serial data line.
(CLKIN)		Input		**External Clock Input** — This pin serves as an external clock input. After reset, the default state is GPIOB6. The peripheral functionality is controlled via the SIM (See **Section 6.3.16**) and the CLKMODE bit of the OCCS Oscillator Control Register.
[11]The SDA signal is also brought out on the GPIOB1 pin.				
GPIOB7	3	Input/ Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(TXD0)		Input/ Output		**Transmit Data 0** — QSCI0 transmit data output or transmit/receive in single wire operation.
(SCL[12])		Input/ Output		**Serial Clock** — This pin serves as the I^2C serial clock. After reset, the default state is GPIOB7. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[12]The SCL signal is also brought out on the GPIOB0 pin.				
GPIOC0	12	Input/ Output	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(ANA0 & CMPAI3)		Analog Input		**ANA0** — Analog input to ADC A, Channel 0. **Comparator A, Input 3** — This is an analog input to Comparator A. When used as an analog input, the signal goes to both the ANA0 and CMPAI3. After reset, the default state is GPIOC0.

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Table 2-3 56F8023 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOC1 **(ANA1)**	11	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANA1** — Analog input to ADC A, Channel 1. After reset, the default state is GPIOC1.
GPIOC2 **(ANA2)** **(V_{REFHA})**	10	Input/ Output Analog Input Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANA2** — Analog input to ADC A, Channel 2. **V_{REFHA}** — Analog reference voltage high (ADC A). After reset, the default state is GPIOC2.
GPIOC4 **(ANB0 & CMPBI3)**	5	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB0** — Analog input to ADC B, Channel 0. **Comparator B, Input 3** — This is an analog input to Comparator B. When used as an analog input, the signal goes to both the ANB0 and CMPBI3. After reset, the default state is GPIOC4.
GPIOC5 **(ANB1)**	6	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB1** — Analog input to ADC B, Channel 1. After reset, the default state is GPIOC5.
GPIOC6 **(ANB2)** **(V_{REFHB})**	7	Input/ Output Analog Input Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB2** — Analog input to ADC B, Channel 2. **V_{REFHB}** — Analog reference voltage high (ADC B). After reset, the default state is GPIOC6.

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Table 2-3 56F8023 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
TDI **(GPIOD0)**	30	Input Input/ Output	Input, internal pull-up enabled	**Test Data Input** — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDI.
TDO **(GPIOD1)**	32	Output Input/ Output	Output, tri-stated, internal pull-up enabled	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TCK **(GPIOD2)**	14	Input Input/ Output	Input, internal pull-up enabled	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-up resistor. A Schmitt trigger input is used for noise immunity. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK.
TMS **(GPIOD3)**	31	Input Input/ Output	Input, internal pull-up enabled	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.

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Part 3 OCCS

3.1 Overview

The On-Chip Clock Synthesis (OCCS) module allows designers using an internal relaxation oscillator, an external crystal, or an external clock to run 56F8000 family devices at user-selectable frequencies up to 32MHz. For details, see the OCCS chapter in the **56F802X and 56F803X Peripheral Reference Manual**.

3.2 Features

The OCCS module interfaces to the oscillator and PLL and offers these features:

- Internal relaxation oscillator
- Ability to power down the internal relaxation oscillator or crystal oscillator
- Ability to put the internal relaxation oscillator into Standby mode
- 3-bit postscaler provides control for the PLL output
- Ability to power down the PLL
- Provides a 2X system clock which operates at twice the system clock to the System Integration Module (SIM)
- Provides a 3X system clock which operates at three times the system clock to PWM and Timer modules
- Safety shutdown feature is available if the PLL reference clock is lost
- Can be driven from an external clock source

The clock generation module provides the programming interface for the PLL, internal relaxation oscillator, and crystal oscillator.

3.3 Operating Modes

In 56F8000 family devices, an internal oscillator, an external crystal, or an external clock source can be used to provide a reference clock to the SIM.

The 2X system clock source output from the OCCS can be described by one of the following equations:

2X system frequency = oscillator frequency

2X system frequency = (oscillator frequency x 8) / (postscaler)

where:

postscaler = 1, 2, 4, 8, 16, or 32

The SIM is responsible for further dividing these frequencies by two, which will insure a 50% duty cycle in the system clock output.

The 56F8000 family devices' on-chip clock synthesis module has the following registers:

- Control Register (OCCS_CTRL)
- Divide-by Register (OCCS_DIVBY)
- Status Register (OCCS_STAT)
- Shutdown Register (OCCS_SHUTDN)
- Oscillator Control Register (OCCS_OCTRL)

For more information on these registers, please refer to the **56F802X and 56F803X Peripheral Reference Manual.**

3.4 Internal Clock Source

An internal relaxation oscillator can supply the reference frequency when an external frequency source or crystal is not used. It is optimized for accuracy and programmability while providing several power-saving configurations which accommodate different operating conditions. The internal relaxation oscillator has very little temperature and voltage variability. To optimize power, the architecture supports a standby state and a power-down state.

During a boot or reset sequence, the relaxation oscillator is enabled by default (the PRECS bit in the PLLCR word is set to 0). Application code can then also switch to the external clock source and power down the internal oscillator, if desired. If a changeover between internal and external clock sources is required at power-on, the user must ensure that the clock source is not switched until the desired external clock source is enabled and stable.

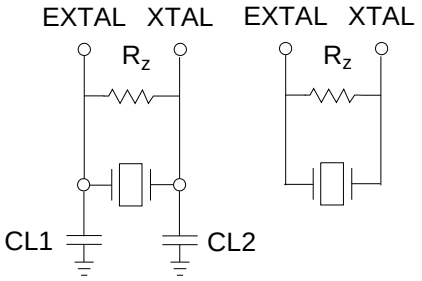
To compensate for variances in the device manufacturing process, the accuracy of the relaxation oscillator can be incrementally adjusted to within $\pm$ 0.078% of 8MHz by trimming an internal capacitor. Bits 0-9 of the OSCTL (oscillator control) register allow the user to set in an additional offset (trim) to this preset value to increase or decrease capacitance. Each unit added or subtracted changes the output frequency by about 0.078% of 8MHz, allowing incremental adjustment until the desired frequency accuracy is achieved.

The center frequency of the internal oscillator is calibrated at the factory to 8MHz and the TRIM value is stored in the Flash information block and loaded to the FMOPT1 register at reset. When using the relaxation oscillator, the boot code should read the FMOPT1 register and set this value as OSCTL TRIM. For further information, see the **56F802X and 56F803X Peripheral Reference Manual**.

3.5 Crystal Oscillator

The internal crystal oscillator circuit is designed to interface with a parallel-resonant crystal resonator in a frequency range of 4-8MHz, specified for the external crystal. **Figure 3-1** shows a typical crystal oscillator circuit. Follow the crystal supplier's recommendations when selecting a crystal, since crystal parameters determine the component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

Crystal Frequency = 4 - 8MHz (optimized for 8MHz)



Sample External Crystal Parameters:
R_z = 750 KΩ

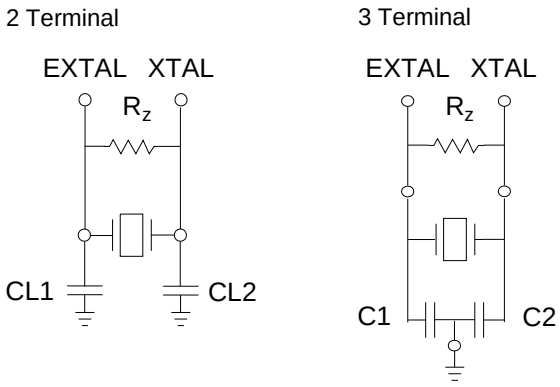
Note: If the operating temperature range is limited to below 85°C (105°C junction), then R_z = 10 Meg Ω

Figure 3-1 External Crystal Oscillator Circuit

3.6 Ceramic Resonator

The internal crystal oscillator circuit is also designed to interface with a ceramic resonator in the frequency range of 4-8MHz. **Figure 3-2** shows the typical 2- and 3-terminal ceramic resonators and their circuits. Follow the resonator supplier's recommendations when selecting a resonator, since their parameters determine the component values required to provide maximum stability and reliable start up. The load capacitance values used in the resonator circuit design should include all stray layout capacitances. The resonator and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

Resonator Frequency = 4 - 8MHz (optimized for 8MHz)



Sample External Ceramic Resonator Parameters:
R_z = 750 KΩ

Figure 3-2 External Ceramic Resonator Circuit

3.7 External Clock Input - Crystal Oscillator Option

The recommended method of connecting an external clock is illustrated in **Figure 3-3.** The external clock source is connected to XTAL and the EXTAL pin is grounded. The external clock input must be generated using a relatively low impedance driver.

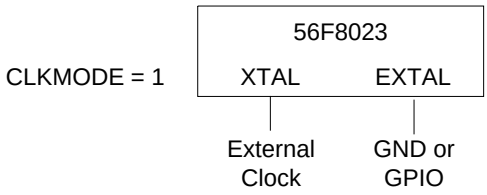


Figure 3-3 Connecting an External Clock Signal using XTAL

3.8 Alternate External Clock Input

The recommended method of connecting an external clock is illustrated in **Figure 3-3.** The external clock source is connected to GPIO6/RXD (primary) or GPIOB5/TA1/FAULT3/XTAL/EXTAL (secondary). The user has the option of using GPIO6/RXD/CLKIN or GPIOB5/TA1/FAULT3/CLKIN as external clock input.

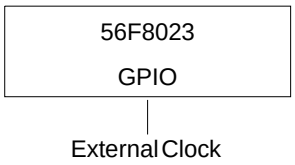


Figure 3-4 Connecting an External Clock Signal using GPIO

Part 4 Memory Maps

4.1 Introduction

The 56F8023 device is a 16-bit motor-control chip based on the 56800E core. It uses a Harvard-style architecture with two independent memory spaces for Data and Program. On-chip RAM is shared by both spaces and Flash memory is used only in Program space.

This section provides memory maps for:

- Program Address Space, including the Interrupt Vector Table
- Data Address Space, including the EOnCE Memory and Peripheral Memory Maps

On-chip memory sizes for the device are summarized in **Table 4-1.** Flash memories' restrictions are identified in the "Use Restrictions" column of **Table 4-1.**

Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8023	Use Restrictions
Program Flash (PFLASH)	16k x 16 or 32KB	Erase / Program via Flash interface unit and word writes to CDBW

Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8023	Use Restrictions
Unified RAM (RAM)	2k x 16 or 4KB	Usable by both the Program and Data memory spaces

4.2 Interrupt Vector Table

Table 4-2 provides the 56F8023's reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. As indicated, the priority of an interrupt can be assigned to different levels, allowing some control over interrupt priorities. All level 3 interrupts will be serviced before level 2, and so on. For a selected priority level, the lowest vector number has the highest priority.

The location of the vector table is determined by the Vector Base Address (VBA). Please see **Section 5.6.8** for the reset value of the VBA.

By default, the chip reset address and COP reset address will correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 4-2 Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
core			P:$00	Reserved for Reset Overlay[2]
core			P:$02	Reserved for COP Reset Overlay
core	2	3	P:$04	Illegal Instruction
core	3	3	P:$06	SW Interrupt 3
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access
core	6	1-3	P:$0C	EOnCE Step Counter
core	7	1-3	P:$0E	EOnCE Breakpoint Unit
core	8	1-3	P:$10	EOnCE Trace Buffer
core	9	1-3	P:$12	EOnCE Transmit Register Empty
core	10	1-3	P:$14	EOnCE Receive Register Full
core	11	2	P:$16	SW Interrupt 2
core	12	1	P:$18	SW Interrupt 1
core	13	0	P:$1A	SW Interrupt 0
	14			Reserved
LVI	15	1-3	P:$1E	Low-Voltage Detector (Power Sense)
PLL	16	1-3	P:$20	Phase-Locked Loop
FM	17	0-2	P:$22	FM Access Error Interrupt

Table 4-2 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
FM	18	0-2	P:$24	FM Command Complete
FM	19	0-2	P:$26	FM Command, Data, and Address Buffers Empty
	20 - 23			Reserved
GPIOD	24	0-2	P:$30	GPIOD
GPIOC	25	0-2	P:$32	GPIOC
GPIOB	26	0-2	P:$34	GPIOB
GPIOA	27	0-2	P:$36	GPIOA
QSPI0	28	0-2	P:$38	QSPI0 Receiver Full
QSPI0	29	0-2	P:$3A	QSPI0 Transmitter Empty
	30 - 31			Reserved
QSCI0	32	0-2	P:$40	QSCI0 Transmitter Empty
QSCI0	33	0-2	P:$42	QSCI0 Transmitter Idle
QSCI0	34	0-2	P:$44	QSCI0 Receiver Error
QSCI0	35	0-2	P:$46	QSCI0 Receiver Full
	36 - 39			Reserved
I2C	40	0-2	P:$50	I^2C Error
I2C	41	0-2	P:$52	I^2C General
I2C	42	0-2	P:$54	I^2C Receive
I2C	43	0-2	P:$56	I^2C Transmit
I2C	44	0-2	P:$58	I^2C Status
TMRA	45	0-2	P:$5A	Timer A, Channel 0
TMRA	46	0-2	P:$5C	Timer A, Channel 1
TMRA	47	0-2	P:$5E	Timer A, Channel 2
TMRA	48	0-2	P:$60	Timer A, Channel 3
	49 - 52			Reserved
CMPA	53	0-2	P:$6A	Comparator A
CMPB	54	0-2	P:$6C	Comparator B
PIT0	55	0-2	P:$6E	Interval Timer 0
	56 - 57			Reserved
ADC	58	0-2	P:$74	ADC A Conversion Complete
ADC	59	0-2	P:$76	ADC B Conversion Complete
ADC	60	0-2	P:$78	ADC Zero Crossing or Limit Error
PWM	61	0-2	P:$7A	Reload PWM
PWM	62	0-2	P:$7C	PWM Fault
SWILP	63	-1	P:$7E	SW Interrupt Low Priority

1. Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.
2. If the VBA is set to the reset value, the first two locations of the vector table will overlay the chip reset addresses since the reset address would match the base of this vector table.

4.3 Program Map

The Program Memory map is shown in **Table 4-3**.

Table 4-3 Program Memory Map[1] at Reset

Begin/End Address	Memory Allocation
P: $1F FFFF P: $00 8800	RESERVED
P: $00 87FF P: $00 8000	On-Chip RAM[2] 4KB
P: $00 7FFF P: $00 4000	Internal Program Flash 32KB Cop Reset Address = $00 4002 Boot Location = $00 4000
P: $00 3FFF P: $00 0000	RESERVED

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Data space starting at address X: $00 0000; see **Figure 4-1**.

4.4 Data Map

Table 4-4 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:$FF FFFF X:$FF FF00	EOnCE 256 locations allocated
X:$FF FEFF X:$01 0000	RESERVED
X:$00 FFFF X:$00 F000	On-Chip Peripherals 4096 locations allocated
X:$00 EFFF X:$00 8800	RESERVED
X:$00 87FF X:$00 8000	RESERVED
X:$00 7FFF X:$00 0800	RESERVED
X:$00 07FF X:$00 0000	On-Chip Data RAM 4KB[2]

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Program space starting at P: $00 8000; see **Figure 4-1**.

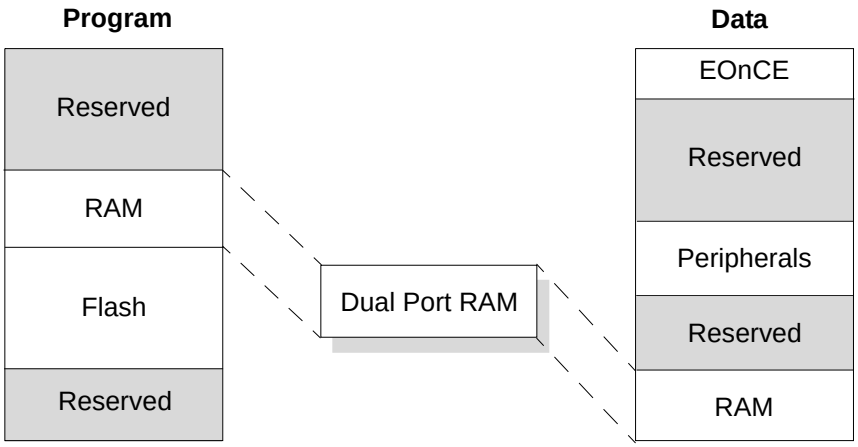


Figure 4-1 Dual Port RAM

4.5 EOnCE Memory Map

Figure 4-5 lists all EOnCE registers necessary to access or control the EOnCE.

Table 4-5 EOnCE Memory Map

Address	Register Acronym	Register Name
X:$FF FFFF	OTX1 / ORX1	Transmit Register Upper Word Receive Register Upper Word
X:$FF FFFE	OTX / ORX (32 bits)	Transmit Register Receive Register
X:$FF FFFD	OTXRXSR	Transmit and Receive Status and Control Register
X:$FF FFFC	OCLSR	Core Lock / Unlock Status Register
X:$FF FFFB - X:$FF FFA1		Reserved
X:$FF FFA0	OCR	Control Register
X:$FF FF9F		Instruction Step Counter
X:$FF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:$FF FF9D	OSR	Status Register
X:$FF FF9C	OBASE	Peripheral Base Address Register
X:$FF FF9B	OTBCR	Trace Buffer Control Register
X:$FF FF9A	OTBPR	Trace Buffer Pointer Register
X:$FF FF99		Trace Buffer Register Stages
X:$FF FF98	OTB (21 - 24 bits/stage)	Trace Buffer Register Stages
X:$FF FF97		Breakpoint Unit Control Register
X:$FF FF96	OBCR (24 bits)	Breakpoint Unit Control Register
X:$FF FF95		Breakpoint Unit Address Register 1
X:$FF FF94	OBAR1 (24 bits)	Breakpoint Unit Address Register 1

Table 4-5 EOnCE Memory Map (Continued)

Address	Register Acronym	Register Name
X:$FF FF93		Breakpoint Unit Address Register 2
X:$FF FF92	OBAR2 (32 bits)	Breakpoint Unit Address Register 2
X:$FF FF91		Breakpoint Unit Mask Register 2
X:$FF FF90	OBMSK (32 bits)	Breakpoint Unit Mask Register 2
X:$FF FF8F		Reserved
X:$FF FF8E	OBCNTR	EOnCE Breakpoint Unit Counter
X:$FF FF8D		Reserved
X:$FF FF8C		Reserved
X:$FF FF8B		Reserved
X:$FF FF8A	OESCR	External Signal Control Register
X:$FF FF89 - X:$FF FF00		Reserved

4.6 Peripheral Memory-Mapped Registers

On-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary Data memory, except all peripheral registers should be read or written using word accesses only.

Table 4-6 summarizes base addresses for the set of peripherals on the 56F8023 device. Peripherals are listed in order of the base address.

The following tables list all of the peripheral registers required to control or access the peripherals.

Table 4-6 Data Memory Peripheral Base Address Map Summary

Peripheral	Prefix	Base Address	Table Number
Timer A	TMRA	X:$00 F000	**4-7**
ADC	ADC	X:$00 F080	**4-8**
PWM	PWM	X:$00 F0C0	**4-9**
ITCN	ITCN	X:$00 F0E0	**4-10**
SIM	SIM	X:$00 F100	**4-11**
COP	COP	X:$00 F120	**4-12**
CLK, PLL, OSC	OCCS	X:$00 F130	**4-13**
Power Supervisor	PS	X:$00 F140	**4-14**
GPIO Port A	GPIOA	X:$00 F150	**4-15**
GPIO Port B	GPIOB	X:$00 F160	**4-16**
GPIO Port C	GPIOC	X:$00 F170	**4-17**
GPIO Port D	GPIOD	X:$00 F180	**4-18**
PIT 0	PIT0	X:$00 F190	**4-19**

Table 4-6 Data Memory Peripheral Base Address Map Summary (Continued)

Peripheral	Prefix	Base Address	Table Number
DAC 0	DAC0	X:$00 F1C0	4-20
DAC 1	DAC1	X:$00 F1D0	4-21
Comparator A	CMPA	X:$00 F1E0	4-22
Comparator B	CMPB	X:$00 F1F0	4-23
QSCI 0	SCI0	X:$00 F200	4-24
QSPI 0	SPI0	X:$00 F220	4-25
I^2C	I2C	X:$00 F280	4-26
FM	FM	X:$00 F400	4-27

Table 4-7 Quad Timer A Registers Address Map (TMRA_BASE = $00 F000)

Register Acronym	Address Offset	Register Description
TMRA0_COMP1	$0	Compare Register 1
TMRA0_COMP2	$1	Compare Register 2
TMRA0_CAPT	$2	Capture Register
TMRA0_LOAD	$3	Load Register
TMRA0_HOLD	$4	Hold Register
TMRA0_CNTR	$5	Counter Register
TMRA0_CTRL	$6	Control Register
TMRA0_SCTRL	$7	Status and Control Register
TMRA0_CMPLD1	$8	Comparator Load Register 1
TMRA0_CMPLD2	$9	Comparator Load Register 2
TMRA0_CSCTRL	$A	Comparator Status and Control Register
TMRA0_FILT	$B	Input Filter Register
		Reserved
TMRA0_ENBL	$F	Timer Channel Enable Register
TMRA1_COMP1	$10	Compare Register 1
TMRA1_COMP2	$11	Compare Register 2
TMRA1_CAPT	$12	Capture Register
TMRA1_LOAD	$13	Load Register
TMRA1_HOLD	$14	Hold Register
TMRA1_CNTR	$15	Counter Register
TMRA1_CTRL	$16	Control Register
TMRA1_SCTRL	$17	Status and Control Register
TMRA1_CMPLD1	$18	Comparator Load Register 1
TMRA1_CMPLD2	$19	Comparator Load Register 2
TMRA1_CSCTRL	$1A	Comparator Status and Control Register

Table 4-7 Quad Timer A Registers Address Map (Continued) (TMRA_BASE = $00 F000)

Register Acronym	Address Offset	Register Description
TMRA1_FILT	$1B	Input Filter Register
		Reserved
TMRA2_COMP1	$20	Compare Register 1
TMRA2_COMP2	$21	Compare Register 2
TMRA2_CAPT	$22	Capture Register
TMRA2_LOAD	$23	Load Register
TMRA2_HOLD	$24	Hold Register
TMRA2_CNTR	$25	Counter Register
TMRA2_CTRL	$26	Control Register
TMRA2_SCTRL	$27	Status and Control Register
TMRA2_CMPLD1	$28	Comparator Load Register 1
TMRA2_CMPLD2	$29	Comparator Load Register 2
TMRA2_CSCTRL	$2A	Comparator Status and Control Register
TMRA2_FILT	$2B	Input Filter Register
		Reserved
TMRA3_COMP1	$30	Compare Register 1
TMRA3_COMP2	$31	Compare Register 2
TMRA3_CAPT	$32	Capture Register
TMRA3_LOAD	$33	Load Register
TMRA3_HOLD	$34	Hold Register
TMRA3_CNTR	$35	Counter Register
TMRA3_CTRL	$36	Control Register
TMRA3_SCTRL	$37	Status and Control Register
TMRA3_CMPLD1	$38	Comparator Load Register 1
TMRA3_CMPLD2	$39	Comparator Load Register 2
TMRA3_CSCTRL	$3A	Comparator Status and Control Register
TMRA3_FILT	$3B	Input Filter Register
		Reserved

Table 4-8 Analog-to-Digital Converter Registers Address Map (ADC_BASE = $00 F080)

Register Acronym	Address Offset	Register Description
ADC_CTRL1	$0	Control Register 1
ADC_CTRL2	$1	Control Register 2
ADC_ZXCTRL	$2	Zero Crossing Control Register
ADC_CLIST 1	$3	Channel List Register 1

Table 4-8 Analog-to-Digital Converter Registers Address Map (Continued) (ADC_BASE = $00 F080)

Register Acronym	Address Offset	Register Description
ADC_CLIST 2	$4	Channel List Register 2
ADC_CLIST 3	$5	Channel List Register 3
ADC_CLIST 4	$6	Channel List Register 4
ADC_SDIS	$7	Sample Disable Register
ADC_STAT	$8	Status Register
ADC_RDY	$9	Conversion Ready Register
ADC_LIMSTAT	$A	Limit Status Register
ADC_ZXSTAT	$B	Zero Crossing Status Register
ADC_RSLT0	$C	Result Register 0
ADC_RSLT1	$D	Result Register 1
ADC_RSLT2	$E	Result Register 2
ADC_RSLT3	$F	Result Register 3
ADC_RSLT4	$10	Result Register 4
ADC_RSLT5	$11	Result Register 5
ADC_RSLT6	$12	Result Register 6
ADC_RSLT7	$13	Result Register 7
ADC_RSLT8	$14	Result Register 8
ADC_RSLT9	$15	Result Register 9
ADC_RSLT10	$16	Result Register 10
ADC_RSLT11	$17	Result Register 11
ADC_RSLT12	$18	Result Register 12
ADC_RSLT13	$19	Result Register 13
ADC_RSLT14	$1A	Result Register 14
ADC_RSLT15	$1B	Result Register 15
ADC_LOLIM0	$1C	Low Limit Register 0
ADC_LOLIM1	$1D	Low Limit Register 1
ADC_LOLIM2	$1E	Low Limit Register 2
ADC_LOLIM3	$1F	Low Limit Register 3
ADC_LOLIM4	$20	Low Limit Register 4
ADC_LOLIM5	$21	Low Limit Register 5
ADC_LOLIM6	$22	Low Limit Register 6
ADC_LOLIM7	$23	Low Limit Register 7
ADC_HILIM0	$24	High Limit Register 0
ADC_HILIM1	$25	High Limit Register 1
ADC_HILIM2	$26	High Limit Register 2
ADC_HILIM3	$27	High Limit Register 3

Table 4-8 Analog-to-Digital Converter Registers Address Map (Continued) (ADC_BASE = $00 F080)

Register Acronym	Address Offset	Register Description
ADC_HILIM4	$28	High Limit Register 4
ADC_HILIM5	$29	High Limit Register 5
ADC_HILIM6	$2A	High Limit Register 6
ADC_HILIM7	$2B	High Limit Register 7
ADC_OFFST0	$2C	Offset Register 0
ADC_OFFST1	$2D	Offset Register 1
ADC_OFFST2	$2E	Offset Register 2
ADC_OFFST3	$2F	Offset Register 3
ADC_OFFST4	$30	Offset Register 4
ADC_OFFST5	$31	Offset Register 5
ADC_OFFST6	$32	Offset Register 6
ADC_OFFST7	$33	Offset Register 7
ADC_PWR	$34	Power Control Register
ADC_CAL	$35	Calibration Register
		Reserved

Table 4-9 Pulse Width Modulator Registers Address Map (PWM_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
PWM_CTRL	$0	Control Register
PWM_FCTRL	$1	Fault Control Register
PWM_FLTACK	$2	Fault Status Acknowledge Register
PWM_OUT	$3	Output Control Register
PWM_CNTR	$4	Counter Register
PWM_CMOD	$5	Counter Modulo Register
PWM_VAL0	$6	Value Register 0
PWM_VAL1	$7	Value Register 1
PWM_VAL2	$8	Value Register 2
PWM_VAL3	$9	Value Register 3
PWM_VAL4	$A	Value Register 4
PWM_VAL5	$B	Value Register 5
PWM_DTIM0	$C	Dead Time Register 0
PWM_DTIM1	$D	Dead Time Register 1
PWM_DMAP1	$E	Disable Mapping Register 1
PWM_DMAP2	$F	Disable Mapping Register 2
PWM_CNFG	$10	Configure Register

Table 4-9 Pulse Width Modulator Registers Address Map (Continued) (PWM_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
PWM_CCTRL	$11	Channel Control Register
PWM_PORT	$12	Port Register
PWM_ICCTRL	$13	Internal Correction Control Register
PWM_SCTRL	$14	Source Control Register
PWM_SYNC	$15	Synchronization Window Register
PWM_FFILT0	$16	Fault0 Filter Register
PWM_FFILT1	$17	Fault1 Filter Register
PWM_FFILT2	$18	Fault2 Filter Register
PWM_FFILT3	$19	Fault3 Filter Register

Table 4-10 Interrupt Control Registers Address Map (ITCN_BASE = $00 F0E0)

Register Acronym	Address Offset	Register Description
ITCN_IPR0	$0	Interrupt Priority Register 0
ITCN_IPR1	$1	Interrupt Priority Register 1
ITCN_IPR2	$2	Interrupt Priority Register 2
ITCN_IPR3	$3	Interrupt Priority Register 3
ITCN_IPR4	$4	Interrupt Priority Register 4
ITCN_IPR5	$5	Interrupt Priority Register 5
ITCN_IPR6	$6	Interrupt Priority Register 6
ITCN_VBA	$7	Vector Base Address Register
ITCN_FIM0	$8	Fast Interrupt Match 0 Register
ITCN_FIVAL0	$9	Fast Interrupt Vector Address Low 0 Register
ITCN_FIVAH0	$A	Fast Interrupt Vector Address High 0 Register
ITCN_FIM1	$B	Fast Interrupt Match 1 Register
ITCN_FIVAL1	$C	Fast Interrupt Vector Address Low 1 Register
ITCN_FIVAH1	$D	Fast Interrupt Vector Address High 1 Register
ITCN_IRQP0	$E	IRQ Pending Register 0
ITCN_IRQP1	$F	IRQ Pending Register 1
ITCN_IRQP2	$10	IRQ Pending Register 2
ITCN_IRQP3	$11	IRQ Pending Register 3
		Reserved
ITCN_ICTRL	$16	Interrupt Control Register
		Reserved

Table 4-11 SIM Registers Address Map (SIM_BASE = $00 F100)

Register Acronym	Address Offset	Register Description
SIM_CTRL	$0	Control Register
SIM_RSTAT	$1	Reset Status Register
SIM_SWC0	$2	Software Control Register 0
SIM_SWC1	$3	Software Control Register 1
SIM_SWC2	$4	Software Control Register 2
SIM_SWC3	$5	Software Control Register 3
SIM_MSHID	$6	Most Significant Half JTAG ID
SIM_LSHID	$7	Least Significant Half JTAG ID
SIM_PWR	$8	Power Control Register
		Reserved
SIM_CLKOUT	$A	Clock Out Select Register
SIM_PCR	$B	Peripheral Clock Rate Register
SIM_PCE0	$C	Peripheral Clock Enable Register 0
SIM_PCE1	$D	Peripheral Clock Enable Register 1
SIM_SD0	$E	Peripheral STOP Disable Register 0
SIM_SD1	$F	Peripheral STOP Disable Register 1
SIM_IOSAHI	$10	I/O Short Address Location High Register
SIM_IOSALO	$11	I/O Short Address Location Low Register
SIM_PROT	$12	Protection Register
SIM_GPSA0	$13	GPIO Peripheral Select Register 0 for GPIOA
		Reserved
SIM_GPSB0	$15	GPIO Peripheral Select Register 0 for GPIOB
SIM_GPSB1	$16	GPIO Peripheral Select Register 1 for GPIOB
		Reserved
SIM_ISS0	$18	Internal Source Select Register 0 for PWM
SIM_ISS1	$19	Internal Source Select Register 1 for DACs
SIM_ISS2	$1A	Internal Source Select Register 2 for TMRA
		Reserved

Table 4-12 Computer Operating Properly Registers Address Map (COP_BASE = $00 F120)

Register Acronym	Address Offset	Register Description
COP_CTRL	$0	Control Register
COP_TOUT	$1	Time-Out Register

Table 4-12 Computer Operating Properly Registers Address Map (COP_BASE = $00 F120)

Register Acronym	Address Offset	Register Description
COP_CNTR	$2	Counter Register

Table 4-13 Clock Generation Module Registers Address Map (OCCS_BASE = $00 F130)

Register Acronym	Address Offset	Register Description
OCCS_CTRL	$0	Control Register
OCCS_DIVBY	$1	Divide-By Register
OCCS_STAT	$2	Status Register
		Reserved
OCCS_OCTRL	$5	Oscillator Control Register
OCCS_CLKCHK	$6	Clock Check Register
OCCS_PROT	$7	Protection Register

Table 4-14 Power Supervisor Registers Address Map (PS_BASE = $00 F140)

Register Acronym	Address Offset	Register Description
PS_CTRL	$0	Control Register
PS_STAT	$1	Status Register
		Reserved

Table 4-15 GPIOA Registers Address Map (GPIOA_BASE = $00 F150)

Register Acronym	Address Offset	Register Description
GPIOA_PUPEN	$0	Pull-up Enable Register
GPIOA_DATA	$1	Data Register
GPIOA_DDIR	$2	Data Direction Register
GPIOA_PEREN	$3	Peripheral Enable Register
GPIOA_IASSRT	$4	Interrupt Assert Register
GPIOA_IEN	$5	Interrupt Enable Register
GPIOA_IEPOL	$6	Interrupt Edge Polarity Register
GPIOA_IPEND	$7	Interrupt Pending Register
GPIOA_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOA_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOA_RDATA	$A	Raw Data Input Register
GPIOA_DRIVE	$B	Output Drive Strength Control Register

Table 4-16 GPIOB Registers Address Map (GPIOB_BASE = $00 F160)

Register Acronym	Address Offset	Register Description
GPIOB_PUPEN	$0	Pull-up Enable Register
GPIOB_DATA	$1	Data Register
GPIOB_DDIR	$2	Data Direction Register
GPIOB_PEREN	$3	Peripheral Enable Register
GPIOB_IASSRT	$4	Interrupt Assert Register
GPIOB_IEN	$5	Interrupt Enable Register
GPIOB_IEPOL	$6	Interrupt Edge Polarity Register
GPIOB_IPEND	$7	Interrupt Pending Register
GPIOB_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOB_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOB_RDATA	$A	Raw Data Input Register
GPIOB_DRIVE	$B	Output Drive Strength Control Register

Table 4-17 GPIOC Registers Address Map (GPIOC_BASE = $00 F170)

Register Acronym	Address Offset	Register Description
GPIOC_PUPEN	$0	Pull-up Enable Register
GPIOC_DATA	$1	Data Register
GPIOC_DDIR	$2	Data Direction Register
GPIOC_PEREN	$3	Peripheral Enable Register
GPIOC_IASSRT	$4	Interrupt Assert Register
GPIOC_IEN	$5	Interrupt Enable Register
GPIOC_IEPOL	$6	Interrupt Edge Polarity Register
GPIOC_IPEND	$7	Interrupt Pending Register
GPIOC_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOC_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOC_RDATA	$A	Raw Data Input Register
GPIOC_DRIVE	$B	Output Drive Strength Control Register

Table 4-18 GPIOD Registers Address Map (GPIOD_BASE = $00 F180)

Register Acronym	Address Offset	Register Description
GPIOD_PUPEN	$0	Pull-up Enable Register
GPIOD_DATA	$1	Data Register
GPIOD_DDIR	$2	Data Direction Register
GPIOD_PEREN	$3	Peripheral Enable Register
GPIOD_IASSRT	$4	Interrupt Assert Register
GPIOD_IEN	$5	Interrupt Enable Register
GPIOD_IEPOL	$6	Interrupt Edge Polarity Register
GPIOD_IPEND	$7	Interrupt Pending Register
GPIOD_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOD_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOD_RDATA	$A	Raw Data Input Register
GPIOD_DRIVE	$B	Output Drive Strength Control Register

Table 4-19 Programmable Interval Timer 0 Registers Address Map (PIT0_BASE = $00 F190)

Register Acronym	Address Offset	Register Description
PIT0_CTRL	$0	Control Register
PIT0_MOD	$1	Modulo Register
PIT0_CNTR	$2	Counter Register

Table 4-20 Digital-to-Analog Converter 0 Registers Address Map (DAC0_BASE = $00 F1C0)

Register Acronym	Address Offset	Register Description
DAC0_CTRL	$0	Control Register
DAC0_DATA	$1	Data Register
DAC0_STEP	$2	Step Register
DAC0_MINVAL	$3	Minimum Value Register
DAC0_MAXVAL	$4	Maximum Value Register

Table 4-21 Digital-to-Analog Converter 0 Registers Address Map (DAC0_BASE = $00 F1C0)

Register Acronym	Address Offset	Register Description
DAC0_CTRL	$0	Control Register
DAC0_DATA	$1	Data Register
DAC0_STEP	$2	Step Register
DAC0_MINVAL	$3	Minimum Value Register
DAC0_MAXVAL	$4	Maximum Value Register

Table 4-22 Comparator A Registers Address Map (CMPA_BASE = $00 F1E0)

Register Acronym	Address Offset	Register Description
CMPA_CTRL	$0	Control Register
CMPA_STAT	$1	Status Register
CMPA_FILT	$2	Filter Register

Table 4-23 Comparator B Registers Address Map (CMPB_BASE = $00 F1F0)

Register Acronym	Address Offset	Register Description
CMPB_CTRL	$0	Control Register
CMPB_STAT	$1	Status Register
CMPB_FILT	$2	Filter Register

Table 4-24 Queued Serial Communication Interface 0 Registers Address Map (QSCI0_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
QSCI0_RATE	$0	Baud Rate Register
QSCI0_CTRL1	$1	Control Register 1
QSCI0_CTRL2	$2	Control Register 2
QSCI0_STAT	$3	Status Register
QSCI0_DATA	$4	Data Register

Table 4-25 Queued Serial Peripheral Interface 0 Registers Address Map (QSPI0_BASE = $00 F220)

Register Acronym	Address Offset	Register Description
QSPI0_SCTRL	$0	Status and Control Register
QSPI0_DSCTRL	$1	Data Size and Control Register
QSPI0_DRCV	$2	Data Receive Register
QSPI0_DXMIT	$3	Data Transmit Register
QSPI0_FIFO	$4	FIFO Control Register
QSPI0_DELAY	$5	Delay Register

Table 4-26 I^2C Registers Address Map (I2C_BASE = $00 F280)

Register Acronym	Address Offset	Register Description
I2C_CTRL	$0	Control Register
I2C_TAR	$2	Target Address Register
I2C_SAR	$4	Slave Address Register
I2C_DATA	$8	RX/TX Data Buffer and Command Register
I2C_SSHCNT	$A	Standard Speed Clock SCL High Count Register
I2C_SSLCNT	$C	Standard Speed Clock SCL Low Count Register
I2C_FSHCNT	$E	Fast Speed Clock SCL High Count Register
I2C_FSLCNT	$10	Fast Speed Clock SCL Low Count Register
I2C_ISTAT	$16	Interrupt Status Register
I2C_IMASK	$18	Interrupt Mask Register
I2C_RISTAT	$1A	Raw Interrupt Status Register
I2C_RXFT	$1C	Receive FIFO Threshold Register
I2C_TXFT	$1E	Transmit FIFO Threshold Register
I2C_CLRINT	$20	Clear Combined and Individual Interrupts Register
I2C_CLRRXUND	$22	Clear RX_UNDER Interrupt Register
I2C_CLRRXOVR	$24	Clear RX_OVER Interrupt Register
I2C_CLRTXOVR	$26	Clear TX_OVER Interrupt Register
I2C_CLRRDREQ	$28	Clear RD_REQ Interrupt Register
I2C_CLRTXABRT	$2A	Clear TX_ABRT Interrupt Register
I2C_CLRRXDONE	$2C	Clear RX_DONE Interrupt Register
I2C_CLRACT	$2E	Clear Activity Interrupt Register
I2C_CLRSTPDET	$30	Clear STOP_DET Interrupt Register
I2C_CLRSTDET	$32	Clear START_DET Interrupt Register
I2C_CLRGC	$34	Clear GEN_CALL Interrupt Register

Table 4-26 I²C Registers Address Map (Continued) (I2C_BASE = $00 F280)

Register Acronym	Address Offset	Register Description
I2C_ENBL	$36	Enable Register
I2C_STAT	$38	Status Register
I2C_TXFLR	$3A	Transmit FIFO Level Register
I2C_RXFLR	$3C	Receive FIFO Level Register
I2C_TXABRTSRC	$40	Transmit Abort Status Register

Table 4-27 Flash Module Registers Address Map (FM_BASE = $00 F400)

Register Acronym	Address Offset	Register Description
FM_CLKDIV	$0	Clock Divider Register
FM_CNFG	$1	Configuration Register
	$2	Reserved
FM_SECHI	$3	Security High Half Register
FM_SECLO	$4	Security Low Half Register
	$5 - $9	Reserved
FM_PROT	$10	Protection Register
	$11 - $12	Reserved
FM_USTAT	$13	User Status Register
FM_CMD	$14	Command Register
	$15 - $17	Reserved
FM_DATA	$18	Data Buffer Register
	$19 - $A	Reserved
FM_IFROPT_1	$1B	Information Option Register 1
	$1C	Reserved
FM_TSTSIG	$1D	Test Array Signature Register

Part 5 Interrupt Controller (ITCN)

5.1 Introduction

The Interrupt Controller (ITCN) module arbitrates between various interrupt requests (IRQs), signals to the 56800E core when an interrupt of sufficient priority exists, and to what address to jump in order to service this interrupt.

5.2 Features

The ITCN module design includes these distinctive features:

- Programmable priority levels for each IRQ
- Two programmable Fast Interrupts
- Notification to SIM module to restart clocks out of Wait and Stop modes
- Ability to drive initial address on the address bus after reset

For further information, see **Table 4-2**, Interrupt Vector Table Contents.

5.3 Functional Description

The Interrupt Controller is a slave on the IPBus. It contains registers that allow each of the 64 interrupt sources to be set to one of four priority levels (excluding certain interrupts that are of fixed priority). Next, all of the interrupt requests of a given level are priority encoded to determine the lowest numerical value of the active interrupt requests for that level. Within a given priority level, number 0 is the highest priority and number 63 is the lowest.

5.3.1 Normal Interrupt Handling

Once the INTC has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the Vector Base Address (VBA) and the vector number to determine the vector address, generating an offset into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The 56800E core controls the masking of interrupt priority levels it will accept by setting the I0 and I1 bits in its status register.

Table 5-1 Interrupt Mask Bit Definition

SR[9] (I1)	SR[8] (I0)	Exceptions Permitted	Exceptions Masked
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

The IPIC bits of the ICTRL register reflect the state of the priority level being presented to the 56800E core.

Table 5-2 Interrupt Priority Encoding

IPIC_VALUE[1:0]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priority 2 or 3	Priority 3

5.3.3 Fast Interrupt Handling

Fast interrupts are described in the **DSP56800E Reference Manual**. The interrupt controller recognizes Fast Interrupts before the core does.

A Fast Interrupt is defined (to the ITCN) by:

1. Setting the priority of the interrupt as level 2, with the appropriate field in the IPR registers
2. Setting the FIM*n* register to the appropriate vector number
3. Setting the FIVAL*n* and FIVAH*n* registers with the address of the code for the Fast Interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the ITCN handles it as a Fast Interrupt. The ITCN takes the vector address from the appropriate FIVAL*n* and FIVAH*n* registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector address and if it is not a JSR, the core starts its Fast Interrupt handling.

5.4 Block Diagram

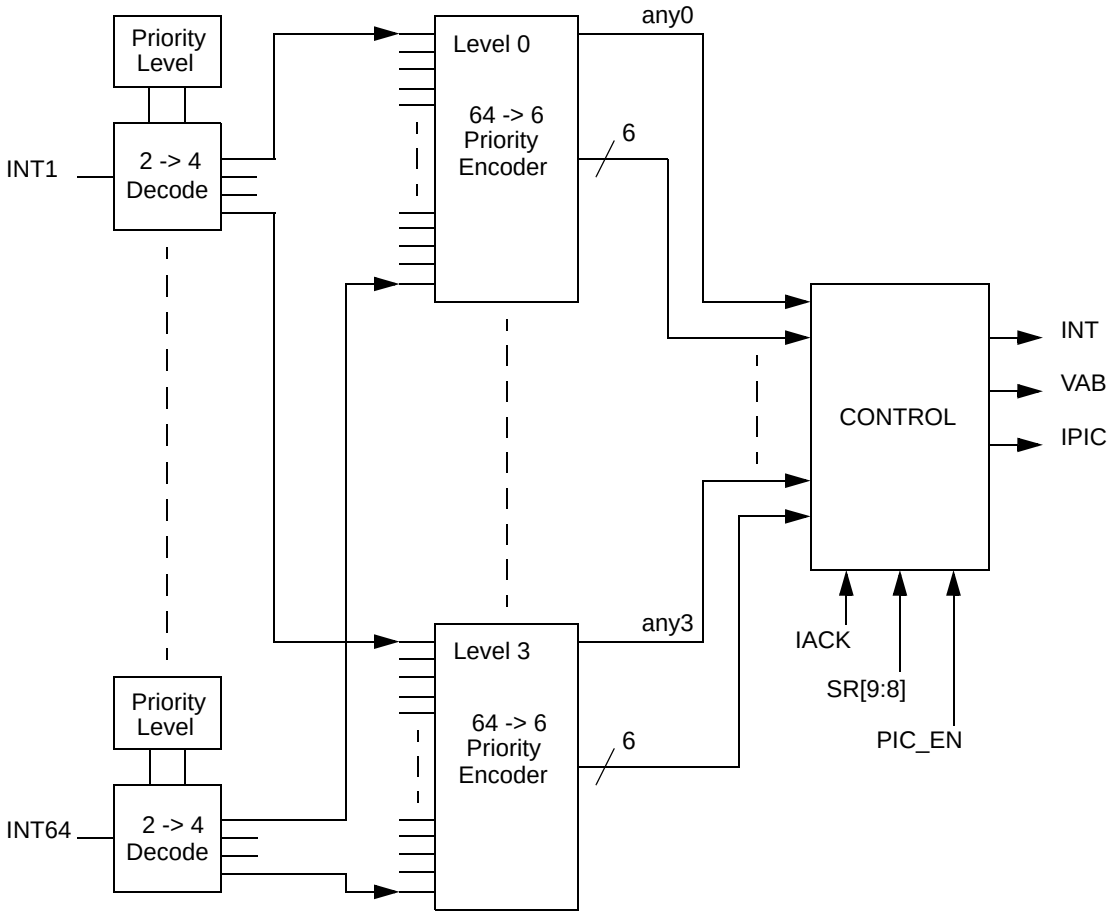


Figure 5-1 Interrupt Controller Block Diagram

5.5 Operating Modes

The ITCN module design contains two major modes of operation:

- **Functional Mode**
  The ITCN is in this mode by default.
- **Wait and Stop Modes**
  During Wait and Stop modes, the system clocks and the 56800E core are turned off. The ITCN will signal a pending IRQ to the System Integration Module (SIM) to restart the clocks and service the IRQ. An IRQ can only wake up the core if the IRQ is enabled prior to entering the Wait or Stop mode.

5.6 Register Descriptions

A register address is the sum of a base address and an address offset. The base address is defined at the system level and the address offset is defined at the module level.

Table 5-3 ITCN Register Summary (ITCN_BASE = $00 F0E0)

Register Acronym	Base Address +	Register Name	Section Location
IPR0	$0	Interrupt Priority Register 0	5.6.1
IPR1	$1	Interrupt Priority Register 1	5.6.2
IPR2	$2	Interrupt Priority Register 2	5.6.3
IPR3	$3	Interrupt Priority Register 3	5.6.4
IPR4	$4	Interrupt Priority Register 4	5.6.5
IPR5	$5	Interrupt Priority Register 5	5.6.6
IPR6	$6	Interrupt Priority Register 6	5.6.7
VBA	$7	Vector Base Address Register	5.6.8
FIM0	$8	Fast Interrupt Match 0 Register	5.6.9
FIVAL0	$9	Fast Interrupt 0 Vector Address Low Register	5.6.10
FIVAH0	$A	Fast Interrupt 0 Vector Address High 0 Register	5.6.11
FIM1	$B	Fast Interrupt Match 1 Register	5.6.12
FIVAL1	$C	Fast Interrupt 1 Vector Address Low Register	5.6.13
FIVAH1	$D	Fast Interrupt 1 Vector Address High Register	5.6.14
IRQP0	$E	IRQ Pending Register 0	5.6.15
IRQP1	$F	IRQ Pending Register 1	5.6.16
IRQP2	$10	IRQ Pending Register 2	5.6.17
IRQP3	$11	IRQ Pending Register 3	5.6.18
		Reserved	
ICTRL	$16	Interrupt Control Register	5.6.19
		Reserved	

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	PLL IPL		LVI IPL		0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL		BKPT_U IPL		STPCNT IPL	
		W																
$1	IPR1	R	GPIOD IPL		0	0	0	0	0	0	0	0	FM_CBE IPL		FM_CC IPL		FM_ERR IPL	
		W																
$2	IPR2	R	QSCI0_XMIT IPL		0	0	0	0	QSPI0_XMIT IPL		QSPI0_RCV IPL		GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$3	IPR3	R	I2C_ERR IPL		0	0	0	0	0	0	0	0	QSCI0_RCV IPL		QSCI0_RERR IPL		QSCI0_TIDL IPL	
		W																
$4	IPR4	R	TMRA_3 IPL		TMRA_2 IPL		TMRA_1 IPL		TMRA_0 IPL		I2C_STAT IPL		I2C_TX IPL		I2C_RX IPL		I2C_GEN IPL	
		W																
$5	IPR5	R	0	0	PIT0 IPL		COMPB IPL		COMPA IPL		0	0	0	0	0	0	0	0
		W																
$6	IPR6		0	0	0	0	PWM_F IPL		PWM_RL IPL		ADC_ZC IPL		ADCB_CC IPL		ADCA_CC IPL		0	0
$7	VBA	R	0	0	VECTOR_BASE_ADDRESS													
		W																
$8	FIM0	R	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0					
		W																
$9	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$A	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$B	FIM1	R	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1					
		W																
$C	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$D	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W																
$E	IRQP0	R	PENDING[16:2]															1
		W																
$F	IRQP1	R	PENDING[32:17]															
		W																
$10	IRQP2	R	PENDING[48:33]															
		W																
$11	IRQP3	R	PENDING[63:49]															
		W																
	Reserved																	
$16	ICTRL	R	INT	IPIC			VAB						INT_ DIS	1	1	1	0	0
		W																
	Reserved																	

= Reserved

Figure 5-2 ITCN Register Map Summary

5.6.1 Interrupt Priority Register 0 (IPR0)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PLL IPL		LVI IPL		0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL		BKPT_U IPL		STPCNT IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-3 Interrupt Priority Register 0 (IPR0)

5.6.1.1 PLL Loss of Reference or Change in Lock Status Interrupt Priority Level (PLL IPL)—Bits 15–14

This field is used to set the interrupt priority levels for the PLL Loss of Reference or Change in Lock Status IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.2 Low Voltage Detector Interrupt Priority Level (LVI IPL)—Bits 13–12

This field is used to set the interrupt priority levels for the Low Voltage Detector IRQ. This IRQ is limited to priorities 1 through 3 and is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.3 Reserved—Bits 11–10

This bit field is reserved. Each bit must be set to 0.

5.6.1.4 EOnCE Receive Register Full Interrupt Priority Level (RX_REG IPL)— Bits 9–8

This field is used to set the interrupt priority level for the EOnCE Receive Register Full IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.5 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)— Bits 7–6

This field is used to set the interrupt priority level for the EOnCE Transmit Register Empty IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.6 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)— Bits 5–4

This field is used to set the interrupt priority level for the EOnCE Trace Buffer IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.7 EOnCE Breakpoint Unit Interrupt Priority Level (BKPT_U IPL)— Bits 3–2

This field is used to set the interrupt priority level for the EOnCE Breakpoint Unit IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.8 EOnCE Step Counter Interrupt Priority Level (STPCNT IPL)— Bits 1–0

This field is used to set the interrupt priority level for the EOnCE Step Counter IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2 Interrupt Priority Register 1 (IPR1)

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	GPIOD IPL		0	0	0	0	0	0	0	0	FM_CBE IPL		FM_CC IPL		FM_ERR IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-4 Interrupt Priority Register 1 (IPR1)

5.6.2.1 GPIOD Interrupt Priority Level (GPIOD IPL)—Bits 15–14

This field is used to set the interrupt priority level for the GPIOD IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.2.2 Reserved—Bits 13–6

This bit field is reserved. Each bit must be set to 0.

5.6.2.3 FM Command, Data, Address Buffers Empty Interrupt Priority Level (FM_CBE IPL)—Bits 5–4

This field is used to set the interrupt priority level for the FM Command, Data Address Buffers Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.2.4 FM Command Complete Interrupt Priority Level (FM_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for the FM Command Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.2.5 FM Error Interrupt Priority Level (FM_ERR IPL)—Bits 1–0

This field is used to set the interrupt priority level for the FM Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3 Interrupt Priority Register 2 (IPR2)

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	QSCI0_XMIT IPL		0	0	0	0	QSPI0_XMIT IPL		QSPI0_RCV IPL		GPIOA IPL		GPIOB IPL		GPIOC IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-5 Interrupt Priority Register 2 (IPR2)

5.6.3.1 QSCI 0 Transmitter Empty Interrupt Priority Level (QSCI0_XMIT IPL)—Bits 15–14

This field is used to set the interrupt priority level for the QSCI0 Transmitter Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.2 Reserved—Bits 13–10

This bit field is reserved. Each bit must be set to 0.

5.6.3.3 QSPI 0 Transmitter Empty Interrupt Priority Level (QSPI0_XMIT IPL)—Bits 9–8

This field is used to set the interrupt priority level for the QSPI0 Transmitter Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.4 QSPI 0 Receiver Full Interrupt Priority Level (QSPI0_RCV IPL)—Bits 7–6

This field is used to set the interrupt priority level for the QSPI0 Receiver Full IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.5 GPIOA Interrupt Priority Level (GPIOA IPL)—Bits 5–4

This field is used to set the interrupt priority level for the GPIOA IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.6 GPIOB Interrupt Priority Level (GPIOB IPL)—Bits 3–2

This field is used to set the interrupt priority level for the GPIOB IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.7 GPIOC Interrupt Priority Level (GPIOC IPL)—Bits 1–0

This field is used to set the interrupt priority level for the GPIOC IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4 Interrupt Priority Register 3 (IPR3)

Base + $3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	I2C_ERR IPL		0	0	0	0	0	0	0	0	QSCI0_RCV IPL		QSCI0_RERR IPL		QSCI0_TIDL IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-6 Interrupt Priority Register 3 (IPR3)

5.6.4.1 I^2C Error Interrupt Priority Level (I2C_ERR IPL)—Bits 15–14

This field is used to set the interrupt priority level for the I^2C Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.2 Reserved—Bits 13–6

This bit field is reserved. Each bit must be set to 0.

5.6.4.3 QSCI 0 Receiver Full Interrupt Priority Level (QSCI0_RCV IPL)—Bits 5–4

This field is used to set the interrupt priority level for the QSCI0 Receiver Full IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.4 QSCI 0 Receiver Error Interrupt Priority Level (QSCI0_RERR IPL)—Bits 3–2

This field is used to set the interrupt priority level for the QSCI0 Receiver Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.5 QSCI 0 Transmitter Idle Interrupt Priority Level (QSCI0_TIDL IPL)—Bits 1–0

This field is used to set the interrupt priority level for the QSCI0 Transmitter Idle IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5 Interrupt Priority Register 4 (IPR4)

Base + $4	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRA_3 IPL		TMRA_2 IPL		TMRA_1 IPL		TMRA_0 IPL		I2C_STAT IPL		I2C_TX IPL		I2C_RX IPL		I2C_GEN IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-7 Interrupt Priority Register 4 (IPR4)

5.6.5.1 Timer A, Channel 3 Interrupt Priority Level (TMRA_3 IPL)—Bits 15–14

This field is used to set the interrupt priority level for the Timer A, Channel 3 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.2 Timer A, Channel 2 Interrupt Priority Level (TMRA_2 IPL)—Bits 13–12

This field is used to set the interrupt priority level for the Timer A, Channel 2 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.3 Timer A, Channel 1 Interrupt Priority Level (TMRA_1 IPL)—Bits 11–10

This field is used to set the interrupt priority level for the Timer A, Channel 1 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.4 Timer A, Channel 0 Interrupt Priority Level (TMRA_0 IPL)—Bits 9–8

This field is used to set the interrupt priority level for the Timer A, Channel 0 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.5 I^2C Status Interrupt Priority Level (I2C_STAT IPL)—Bits 7–6

This field is used to set the interrupt priority level for the I^2C Status IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.6 I^2C Transmit Interrupt Priority Level (I2C_TX IPL)—Bits 5–4

This field is used to set the interrupt priority level for the I^2C Transmit IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.7 I^2C Receive Interrupt Priority Level (I2C_RX IPL)— Bits 3–2

This field is used to set the interrupt priority level for the I^2C Receiver IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.8 I^2C General Call Interrupt Priority Level (I2C_GEN IPL)—Bits 1–0

This field is used to set the interrupt priority level for the I^2C General Call IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6 Interrupt Priority Register 5 (IPR5)

Base + $5	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	PIT0 IPL		COMPB IPL		COMPA IPL		0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-8 Interrupt Priority Register 5 (IPR6)

5.6.6.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

5.6.6.2 Programmable Interval Timer 0 Interrupt Priority Level (PIT0 IPL)—Bits 13–12

This field is used to set the interrupt priority level for the Programmable Interval Timer 0 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.3 Comparator B Interrupt Priority Level (COMPB IPL)—Bits 11–10

This field is used to set the interrupt priority level for the Comparator B IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.4 Comparator A Interrupt Priority Level (COMPA IPL)—Bits 9–8

This field is used to set the interrupt priority level for the Comparator IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.5 Reserved—Bits 7–0

This bit field is reserved. Each bit must be set to 0.

5.6.7 Interrupt Priority Register 6 (IPR6)

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	PWM_F IPL		PWM_RL IPL		ADC_ZC IPL		ADCB_CC IPL		ADCA_CC IPL		0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-9 Interrupt Priority Register 6 (IPR6)

5.6.7.1 Reserved—Bits 15–12

This bit field is reserved. Each bit must be set to 0.

5.6.7.2 PWM Fault Interrupt Priority Level (PWM_F IPL)—Bits 11–10

This field is used to set the interrupt priority level for the PWM Fault Interrupt IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.3 Reload PWM Interrupt Priority Level (PWM_RL IPL)—Bits 9–8

This field is used to set the interrupt priority level for the Reload PWM Interrupt IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.4 ADC Zero Crossing Interrupt Priority Level (ADC_ZC IPL)—Bits 7–6

This field is used to set the interrupt priority level for the ADC Zero Crossing IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.5 ADC B Conversion Complete Interrupt Priority Level (ADCB_CC IPL)—Bits 5–4

This field is used to set the interrupt priority level for the ADC B Conversion Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.6 ADC A Conversion Complete Interrupt Priority Level (ADCA_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for the ADC A Conversion Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.7 Reserved—Bits 1–0

This bit field is reserved. Each bit must be set to 0.

5.6.8 Vector Base Address Register (VBA)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	VECTOR_BASE_ADDRESS													
Write																
RESET[1]	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

1. The 56F8023 resets to a value of 0 x 0080. This corresponds to reset addresses of 0 x 004000.

Figure 5-10 Vector Base Address Register (VBA)

5.6.8.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

5.6.8.2 Vector Address Bus (VAB) Bits 13–0

The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower 7 bits are determined based on the highest priority interrupt and are then appended onto VBA before presenting the full VAB to the Core.

5.6.9 Fast Interrupt Match 0 Register (FIM0)

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0					
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-11 Fast Interrupt Match 0 Register (FIM0)

5.6.9.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

5.6.9.2 Fast Interrupt 0 Vector Number (FAST INTERRUPT 0)—Bits 5–0

These values determine which IRQ will be Fast Interrupt 0. Fast Interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first. IRQs used as Fast Interrupts *must* be set to priority level 2. Unexpected results will occur if a Fast Interrupt vector is set to any other priority. A Fast Interrupt automatically becomes the highest-priority level 2 interrupt regardless of its location in the interrupt table prior to being declared as Fast Interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to the vector table.

5.6.10 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

Base + $9	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-12 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

5.6.10.1 Fast Interrupt 0 Vector Address Low (FIVAL0)—Bits 15–0

The lower 16 bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAH0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.11 Fast Interrupt 0 Vector Address High Register (FIVAH0)

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-13 Fast Interrupt 0 Vector Address High Register (FIVAH0)

5.6.11.1 Reserved—Bits 15–5

This bit field is reserved. Each bit must be set to 0.

5.6.11.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.12 Fast Interrupt 1 Match Register (FIM1)

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1					
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-14 Fast Interrupt 1 Match Register (FIM1)

5.6.12.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

5.6.12.2 Fast Interrupt 1 Vector Number (FAST INTERRUPT 1)—Bits 5–0

These values determine which IRQ will be Fast Interrupt 1. Fast Interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first. IRQs used as Fast Interrupts *must* be set to priority level 2. Unexpected results will occur if a Fast Interrupt vector is set to any other priority. A Fast Interrupt automatically becomes the highest priority level 2 interrupt, regardless of its location in the interrupt table prior to being declared as Fast Interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to the vector table.

5.6.13 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-15 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

5.6.13.1 Fast Interrupt 1 Vector Address Low (FIVAL1)—Bits 15–0

The lower 16 bits of the vector address used for Fast Interrupt 1. This register is combined with FIVAH1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.14 Fast Interrupt 1 Vector Address High (FIVAH1)

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-16 Fast Interrupt 1 Vector Address High Register (FIVAH1)

5.6.14.1 Reserved—Bits 15–5

This bit field is reserved. Each bit must be set to 0.

5.6.14.2 Fast Interrupt 1 Vector Address High (FIVAH1)—Bits 4–0

The upper five bits of the vector address used for Fast Interrupt 1. This register is combined with FIVAL1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.15 IRQ Pending Register 0 (IRQP0)

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING[16:2]															1
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-17 IRQ Pending Register 0 (IRQP0)

5.6.15.1 IRQ Pending (PENDING)—Bits 16–2

These register bit values represent the pending IRQs for interrupt vector numbers 2 through 16. Ascending IRQ numbers correspond to ascending bit locations.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.15.2 Reserved—Bit 0

This bit field is reserved. It must be set to 1.

5.6.16 IRQ Pending Register 1 (IRQP1)

Base + $F	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING[32:17]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-18 IRQ Pending Register 1 (IRQP1)

5.6.16.1 IRQ Pending (PENDING)—Bits 32–17

These register bit values represent the pending IRQs for interrupt vector numbers 17 through 32. Ascending IRQ numbers correspond to ascending bit locations.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.17 IRQ Pending Register 2 (IRQP2)

Base + $10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING[48:33]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-19 IRQ Pending Register 2 (IRQP2)

5.6.17.1 IRQ Pending (PENDING)—Bits 48–33

This register bit values represent the pending IRQs for interrupt vector numbers 33 through 48. Ascending IRQ numbers correspond to ascending bit locations.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.18 IRQ Pending Register 3 (IRQP3)

Base + $11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING[63:49]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-20 IRQ Pending Register 3 (IRQP3)

5.6.18.1 IRQ Pending (PENDING)—Bits 63–49

These register bit values represent the pending IRQs for interrupt vector numbers 49 through 63. Ascending IRQ numbers correspond to ascending bit locations.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.19 Interrupt Control Register (ICTRL)

$Base + $16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	INT	IPIC		VAB							INT_DIS	1	1	1	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

Figure 5-21 Interrupt Control Register (ICTRL)

5.6.19.1 Interrupt (INT)—Bit 15

This *read-only* bit reflects the state of the interrupt to the 56800E core.

- 0 = No interrupt is being sent to the 56800E core
- 1 = An interrupt is being sent to the 56800E core

5.6.19.2 Interrupt Priority Level (IPIC)—Bits 14–13

These *read-only* bits reflect the state of the new interrupt priority level bits being presented to the 56800E core. These bits indicate the priority level needed for a new IRQ to interrupt the current interrupt being sent to the 56800E core. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

- 00 = Required nested exception priority levels are 0, 1, 2, or 3
- 01 = Required nested exception priority levels are 1, 2, or 3
- 10 = Required nested exception priority levels are 2 or 3
- 11 = Required nested exception priority level is 3

Table 5-4 Interrupt Priority Encoding

IPIC_VALUE[1:0]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priority 2 or 3	Priority 3

5.6.19.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows bits [7:1] of the Vector Address Bus used at the time the last IRQ was taken. In the case of a Fast Interrupt, it shows the lower address bits of the jump address. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

5.6.19.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

5.6.19.5 Reserved—Bits 4-2

This bit field is reserved. Each bit must be set to 1.

5.6.19.6 Reserved—Bits 1–0

This bit field is reserved. Each bit must be set to 0.

5.7 Resets

5.7.1 General

Table 5-5 Reset Summary

Reset	Priority	Source	Characteristics
Core Reset		$\overline{\text{RST}}$	Core reset from the SIM

5.7.2 Description of Reset Operation

5.7.2.1 Reset Handshake Timing

The ITCN provides the 56800E core with a reset vector address on the VAB pins whenever $\overline{\text{RESET}}$ is asserted from the SIM. The reset vector will be presented until the second rising clock edge after $\overline{\text{RESET}}$ is released. The general timing is shown in **Figure 5-22**.

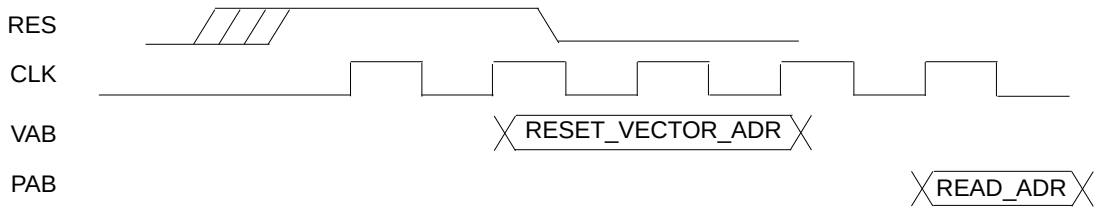


Figure 5-22 Reset Interface

5.7.3 ITCN After Reset

After reset, all of the ITCN registers are in their default states. This means all interrupts are disabled, except the core IRQs with fixed priorities:

- Illegal Instruction
- SW Interrupt 3
- HW Stack Overflow
- Misaligned Long Word Access
- SW Interrupt 2

- SW Interrupt 1
- SW Interrupt 0
- SW Interrupt LP

These interrupts are enabled at their fixed priority levels.

Part 6 System Integration Module (SIM)

6.1 Introduction

The SIM module is a system catchall for the glue logic that ties together the system-on-chip. It controls distribution of resets and clocks and provides a number of control features. The System Integration Module's functions are discussed in more detail in the following sections.

6.2 Features

The SIM has the following features:

- Chip reset sequencing
- Core and peripheral clock control and distribution
- Stop/Wait mode control
- System status control
- Registers containing the JTAG ID of the chip
- Controls for programmable peripheral and GPIO connections
- Peripheral clocks for TMR and PWM with a high-speed (3X) option
- Power-saving clock gating for peripherals
- Three power modes (Run, Wait, Stop) to control power utilization
  - — Stop mode shuts down the 56800E core, system clock, and peripheral clock
  - — Wait mode shuts down the 56800E core and unnecessary system clock operation
  - — Run mode supports full device operation
- Controls the enable/disable functions of the 56800E core WAIT and STOP instructions with write protection capability
- Controls the enable/disable functions of Large Regulator Standby mode with write protection capability
- Permits selected peripherals to run in Stop mode to generate Stop recovery interrupts
- Controls for programmable peripheral and GPIO connections
- Software chip reset
- I/O short address base location control
- Peripheral protection control to provide runaway code protection for safety-critical applications
- Controls output of internal clock sources to CLKO pin
- Four general-purpose software control registers are reset only at power-on
- Peripherals Stop mode clocking control

6.3 Register Descriptions

A write to an address without an associated register is an NOP. A read from an address without an associated register returns unknown data.

Table 6-1 SIM Registers (SIM_BASE = $00 F100)

Register Acronym	Base Address +	Register Name	Section Location
CTRL	$0	Control Register	6.3.1
RSTAT	$1	Reset Status Register	6.3.2
SWC0	$2	Software Control Register 0	6.3.3
SWC1	$3	Software Control Register 1	6.3.3
SWC2	$4	Software Control Register 2	6.3.3
SWC3	$5	Software Control Register 3	6.3.3
MSHID	$6	Most Significant Half of JTAG ID	6.3.4
LSHID	$7	Least Significant Half of JTAG ID	6.3.5
PWR	$8	Power Control Register	6.3.6
		Reserved	
CLKOUT	$A	CLKO Select Register	6.3.7
PCR	$B	Peripheral Clock Rate Register	6.3.8
PCE0	$C	Peripheral Clock Enable Register 0	6.3.9
PCE1	$D	Peripheral Clock Enable Register 0	6.3.10
SD0	$E	Stop Disable Register 0	6.3.11
SD1	$F	Stop Disable Register 1	6.3.12
IOSAHI	$10	I/O Short Address Location High Register	6.3.13
IOSALO	$11	I/O Short Address Location Low Register	6.3.14
PROT	$12	Protection Register	6.3.15
GPSA0	$13	GPIO Peripheral Select Register 0 for GPIOA	6.3.16
		Reserved	
GPSB0	$15	GPIO Peripheral Select Register 0 for GPIOB	6.3.17
GPSB1	$16	GPIO Peripheral Select Register 1 for GPIOB	6.3.18
		Reserved	
ISS0	$18	Internal Source Select Register 0 for PWM	6.3.19
ISS1	$19	Internal Source Select Register 1 for DACs	6.3.20
ISS2	$1A	Internal Source Select Register 2 for Quad Timer A	6.3.21
		Reserved	

Add. Offset	Address Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	SIM_ CTRL	R	0	0	0	0	0	0	0	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
		W																
$1	SIM_ RSTAT	R	0	0	0	0	0	0	0	0	0	SWR	COP_ TOR	COP_ LOR	EXTR	POR	0	0
		W																
$2	SIM_SWC0	R	Software Control Data 0															
		W																
$3	SIM_SWC1	R	Software Control Data 1															
		W																
$4	SIM_SWC2	R	Software Control Data 2															
		W																
$5	SIM_SWC3	R	Software Control Data 3															
		W																
$6	SIM_MSHID	R	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1	0
		W																
$7	SIM_LSHID	R	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
		W																
$8	SIM_PWR	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LRSTDBY	
		W																
	Reserved																	
$A	SIM_ CLKOUT	R	0	0	0	0	0	0	$\overline{\text{PWM3}}$	$\overline{\text{PWM2}}$	$\overline{\text{PWM1}}$	$\overline{\text{PWM0}}$	CLK DIS	CLKOSEL				
		W																
$B	SIM_PCR	R	0	TMRA_ CR	PWM_C R	I2C_ CR	0	0	0	0	0	0	0	0	0	0	0	0
		W																
$C	SIM_PCE0	R	CMPB	CMPA	DAC1	DAC0	0	ADC	0	0	0	I2C	0	QSCI0	0	QSPI0	0	PWM
		W																
$D	SIM_PCE1	R	0	0	0	PIT0	0	0	0	0	0	0	0	0	TA3	TA2	TA1	TA0
		W																
$E	SIM_SD0	R	CMPB_ SD	CMPA_ SD	DAC1_ SD	DAC0_ SD	0	ADC_ SD	0	0	0	I2C_ SD	0	QSCI0 _SD	0	QSPI0 _SD	0	PWM_ SD
		W																
$F	SIM_SD1	R	0	0	0	PIT0_ SD	0	0	0	0	0	0	0	0	TA3_ SD	TA2_ SD	TA1_ SD	TA0_ SD
		W																
$10	SIM_IOSAHI	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ISAL[23:22]	
		W																
$11	SIM_IOSALO	R	ISAL[21:6]															
		W																
$12	SIM_PROT	R	0	0	0	0	0	0	0	0	0	0	0	0	PCEP		GIPSP	
		W																
$13	SIM_GPSA0	R	0	0	0	GPS_ A6	GPS_A5		GPS_A4		0	0	0	0	0	0	0	0
		W																
	Reserved																	
$15	SIM_GPSB0	R	0	GPS_B6		GPS_B5		GPS_B4			GPS_B3		GPS_B2		0	GPS_ B1	0	GPS_ B0
		W																
$16	SIM_GPSB1	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPS_ B7
		W																
	Reserved																	
$18	SIM_IPS0	R	0	0	IPS0_ FAULT2	0	IPS0_ FAULT1	0	0	IPS0_PSRC2			IPS0_PSRC1			IPS0_PSRC0		
		W																
$19	SIM_IPS1	R	0	0	0	0	0	0	0	0	0	0	0	0	0	IPS1_DSYNC0		
		W																
$1A	SIM_IPS2	R	0	0	0	IPS2_ TA3	0	0	0	IPS2_ TA2	0	0	0	IPS2_ TA1	0	0	0	0
		W																
	Reserved																	

0 = Read as 0 1 = Read as 1 = Reserved

Figure 6-1 SIM Register Map Summary

6.3.1 SIM Control Register (SIM_CTRL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-2 SIM Control Register (SIM_CTRL)

6.3.1.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

6.3.1.2 OnCE Enable (ONCEEBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

Note: Using default state “0” is recommended.

6.3.1.3 Software Reset (SWRST)—Bit 4

- Writing 1 to this field will cause the device to reset
- Read is zero

6.3.1.4 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 = Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 = The 56800E STOP instruction will not cause entry into Stop mode
- 10 = Stop mode will be entered when the 56800E core executes a STOP instruction and the STOP_DISABLE field is write-protected until the next reset
- 11 = The 56800E STOP instruction will not cause entry into Stop mode and the STOP_DISABLE field is write-protected until the next reset

6.3.1.5 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 = Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 = The 56800E WAIT instruction will not cause entry into Wait mode
- 10 = Wait mode will be entered when the 56800E core executes a WAIT instruction and the WAIT_DISABLE field is write-protected until the next reset
- 11 = The 56800E WAIT instruction will not cause entry into Wait mode and the WAIT_DISABLE field is write-protected until the next reset

6.3.2 SIM Reset Status Register (SIM_RSTAT)

This read-only register is updated upon any system reset and indicates the cause of the most recent reset. It indicates whether the COP reset vector or regular reset vector (including Power-On Reset, External Reset, Software Reset) in the vector table is used. This register is asynchronously reset during Power-On Reset and subsequently is synchronously updated based on the precedence level of reset inputs. Only the

most recent reset source will be indicated if multiple resets occur. If multiple reset sources assert simultaneously, the highest-precedence source will be indicated. The precedence from highest to lowest is Power-On Reset, External Reset, COP Loss of Reference Reset, COP Time-Out Reset, and Software Reset. Power-On Reset is always set during a Power-On Reset; however, Power-On Reset will be cleared and External Reset will be set if the external reset pin is asserted or remains asserted after the Power-On Reset has deasserted.

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	SWR	COP_ TOR	COP_ LOR	EXTR	POR	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Figure 6-3 SIM Reset Status Register (SIM_RSTAT)

6.3.2.1 Reserved—Bits 15–7

This bit field is reserved. Each bit must be set to 0.

6.3.2.2 Software Reset (SWR)—Bit 6

When set, this bit indicates that the previous system reset occurred as a result of a software reset (written 1 to SWRST bit in the SIM_CTRL register).

6.3.2.3 COP Time-Out Reset (COP_TOR)—Bit 5

When set, this bit indicates that the previous system reset was caused by the Computer Operating Properly (COP) module signaling a COP time-out reset. If COP_TOR is set as code starts executing, the COP reset vector in the vector table will be used. Otherwise, the normal reset vector is used.

6.3.2.4 COP Loss of Reference Reset (COP_LOR)—Bit 4

When set, this bit indicates that the previous system reset was caused by the Computer Operating Properly (COP) module signaling a loss of COP reference clock reset. If COP_LOR is set as code starts executing, the COP reset vector in the vector table will be used. Otherwise, the normal reset vector is used.

6.3.2.5 External Reset (EXTR)—Bit 3

When set, this bit indicates that the previous system reset was caused by an external reset.

6.3.2.6 Power-On Reset (POR)—Bit 2

This bit is set during a Power-On Reset.

6.3.2.7 Reserved—Bits 1–0

This bit field is reserved. Each bit must be set to 0.

6.3.3 SIM Software Control Registers (SIM_SWC0, SIM_SWC1, SIM_SWC2, and SIM_SWC3)

These registers are general-purpose registers. They are reset only at power-on, so they can monitor software execution flow.

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Software Control Data 0 - 3															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-4 SIM Software Control Register 0 (SIM_SWC0 - 3)

6.3.3.1 Software Control Register 0 - 3 (FIELD)—Bits 15–0

This register is reset only by the Power-On Reset (POR). It is intended for use by a software developer to contain data that will be unaffected by the other reset sources (external reset, software reset, and COP reset).

6.3.4 Most Significant Half of JTAG ID (SIM_MSHID)

This read-only register displays the most significant half of the JTAG ID for the chip. This register reads $01F2.

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1	0
Write																
RESET	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1	0

Figure 6-5 Most Significant Half of JTAG ID (SIM_MSHID)

6.3.5 Least Significant Half of JTAG ID (SIM_LSHID)

This read-only register displays the least significant half of the JTAG ID for the chip. This register reads $801D.

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
Write																
RESET	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-6 Least Significant Half of JTAG ID (SIM_LSHID)

6.3.6 SIM Power Control Register (SIM_PWR)

This register controls the Standby mode of the large on-chip regulator. The large on-chip regulator derives the core digital logic power supply from the IO power supply. At a system bus frequency of 200kHz, the large regulator may be put in a reduced-power standby mode without interfering with device operation to reduce device power consumption. Refer to the overview of power-down modes and the overview of clock generation for more information on the use of large regulator standby.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LRSTDBY	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-7 SIM Power Control Register (SIM_PWR)

6.3.6.1 Reserved—Bits 15–2

This bit field is reserved. Each bit must be set to 0.

6.3.6.2 Large Regulator Standby Mode[1:0] (LRSTDBY)—Bits 1–0

- 00 = Large regulator is in Normal mode
- 01 = Large regulator is in Standby (reduced-power) mode
- 10 = Large regulator is in Normal mode and the LRSTDBY field is write-protected until the next reset
- 11 = Large regulator is in Standby mode and the LRSTDBY field is write-protected until the next reset

6.3.7 Clock Output Select Register (SIM_CLKOUT)

The Clock Output Select register can be used to multiplex out selected clock sources generated inside the clock generation and SIM modules onto the muxed clock output pins. All functionality is for test purposes only. Glitches may be produced when the clock is enabled or switched. The delay from the clock source to the output is unspecified. The observability of the CLKO clock output signal at an output pad is subject to the frequency limitations of the associated IO cell.

GPIOA[3:0] can function as GPIO, PWM, or as clock output pins. If GPIOA[3:0] are programmed to operate as peripheral outputs, then the choice is between PWM and clock outputs. The default state is for the peripheral function of GPIOA[3:0] to be programmed as PWM (selected by bits [9:6] of the Clock Output Select register).

GPIOB4 can function as GPIO, or as other peripheral outputs, including clock output (CLKO). If GPIOB4 is programmed to operate as a peripheral output and CLKO is selected in the SIM_GPSB0 register, bits [4:0] decide if CLKO is enabled or disabled and which clock source is selected if CLKO is enabled. See **Figure 6-8** for details.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	$\overline{\text{PWM3}}$	$\overline{\text{PWM2}}$	$\overline{\text{PWM1}}$	$\overline{\text{PWM0}}$	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-8 CLKO Select Register (SIM_CLKOUT)

6.3.7.1 Reserved—Bits 15–10

This bit field is reserved. Each bit must be set to 0.

6.3.7.2 $\overline{\text{PWM3}}$—Bit 9

- 0 = Peripheral output function of GPIOA[3] is defined to be $\overline{\text{PWM3}}$
- 1 = Peripheral output function of GPIOA[3] is defined to be the Relaxation Oscillator Clock

6.3.7.3 $\overline{\text{PWM2}}$—Bit 8

- 0 = Peripheral output function of GPIOA[2] is defined to be $\overline{\text{PWM2}}$
- 1 = Peripheral output function of GPIOA[2] is defined to be the system clock

6.3.7.4 $\overline{\text{PWM1}}$—Bit 7

- 0 = Peripheral output function of GPIOA[1] is defined to be $\overline{\text{PWM1}}$
- 1 = Peripheral output function of GPIOA[1] is defined to be 2X system clock

6.3.7.5 $\overline{\text{PWM0}}$—Bit 6

- 0 = Peripheral output function of GPIOA[0] is defined to be $\overline{\text{PWM0}}$
- 1 = Peripheral output function of GPIOA[0] is defined to be 3X system clock

6.3.7.6 Clockout Disable (CLKDIS)—Bit 5

- 0 = CLKOUT output function is enabled and will output the signal indicated by CLKOSEL
- 1 = CLKOUT output function is disabled

6.3.7.7 Clockout Select (CLKOSEL)—Bits 4–0

CLKOSEL selects the clock to be muxed out on the CLKO pin as defined in the following. Internal delay to CLKO output is unspecified. Signal at the output pad is undefined when CLKO signal frequency exceeds the rated frequency of the I/O cell. CLKO may not operate as expected when CLKDIS and CLKOSEL settings are changed.

- 00000 = Continuous system clock
- 00001 = Continuous peripheral clock
- 00010 = 3X system clock
- 00100.....11111 = Reserved for factory test

6.3.8 Peripheral Clock Rate Register (SIM_PCR)

By default, all peripherals are clocked at the system clock rate, which has a maximum of 32MHz. Selected peripherals clocks have the option to be clocked at 3X system clock rate, which has a maximum of 96MHz, if the PLL output clock is selected as the system clock. If PLL is disabled, the 3X system clock will not be available. This register is used to enable high-speed clocking for those peripherals that support it.

Note: Operation is unpredictable if peripheral clocks are reconfigured at runtime, so peripherals should be disabled before a peripheral clock is reconfigured.

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	TMRA_ CR	PWM_ CR	I2C_ CR	0	0	0	0	0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-9 Peripheral Clock Rate Register (SIM_PCR)

6.3.8.1 Reserved—Bit 15

This bit field is reserved. It must be set to 0.

6.3.8.2 Quad Timer A Clock Rate (TMRA_CR)—Bit 14

This bit selects the clock speed for the Quad Timer A module.

- 0 = Quad Timer A clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = Quad Timer A clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.3 Pulse Width Modulator Clock Rate (PWM_CR)—Bit 13

This bit selects the clock speed for the PWM module.

- 0 = PWM module clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = PWM module clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.4 Inter-Integrated Circuit Run Clock Rate (I2C_CR)—Bit 12

This bit selects the clock speed for the I^2C run clock.

- 0 = I^2C module run clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = I^2C module run clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.5 Reserved—Bits 11–0

This bit field is reserved. Each bit must be set to 0.

6.3.9 Peripheral Clock Enable Register 0 (SIM_PCE0)

The Peripheral Clock Enable register enables or disables clocks to the peripherals as a power savings feature. Significant power savings are achieved by enabling only the peripheral clocks that are in use.

When a peripheral's clock is disabled, that peripheral is in Stop mode. Accesses made to a module that has its clock disabled will have no effect. The corresponding peripheral should itself be disabled while its clock is shut off. IPBus writes are not possible.

Setting the PCE bit does not guarantee that the peripheral's clock is running. Enabled peripheral clocks will still become disabled in Stop mode, unless the peripheral's Stop Disable control in the SD*n* register is set to 1.

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	CMPB	CMPA	DAC1	DAC0	0	ADC	0	0	0	I2C	0	QSCI0	0	QSPI0	0	PWM
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-10 Peripheral Clock Enable Register 0 (SIM_PCE0)

6.3.9.1 Comparator B Clock Enable (CMPB)—Bit 15

- 0 = The clock is not provided to the Comparator B module (the Comparator B module is disabled)
- 1 = The clock is enabled to the Comparator B module

6.3.9.2 Comparator A Clock Enable (CMPA)—Bit 14

- 0 = The clock is not provided to the Comparator A module (the Comparator A module is disabled)
- 1 = The clock is enabled to the Comparator A module

6.3.9.3 Digital-to-Analog Clock Enable 1 (DAC1)—Bit 13

- 0 = The clock is not provided to the DAC1 module (the DAC1 module is disabled)
- 1 = The clock is enabled to the DAC1 module

6.3.9.4 Digital-to-Analog Clock Enable 0 (DAC0)—Bit 12

- 0 = The clock is not provided to the DAC0 module (the DAC0 module is disabled)
- 1 = The clock is enabled to the DAC0 module

6.3.9.5 Reserved—Bit 11

This bit field is reserved. It must be set to 0.

6.3.9.6 Analog-to-Digital Converter Clock Enable (ADC)—Bit 10

- 0 = The clock is not provided to the ADC module (the ADC module is disabled)
- 1 = The clock is enabled to the ADC module

6.3.9.7 Reserved—Bits 9–7

This bit field is reserved. Each bit must be set to 0.

6.3.9.8 Inter-Integrated Circuit IPBus Clock Enable (I2C)—Bit 6

- 0 = The clock is not provided to the I^2C module (the I^2C module is disabled)

- 1 = The clock is enabled to the I^2C module

6.3.9.9 Reserved—Bit 5

This bit field is reserved. It must be set to 0.

6.3.9.10 QSCI 0 Clock Enable (QSCI0)—Bit 4

- 0 = The clock is not provided to the QSCI0 module (the QSCI0 module is disabled)
- 1 = The clock is enabled to the QSCI0 module

6.3.9.11 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.9.12 QSPI 0 Clock Enable (QSPI0)—Bit 2

- 0 = The clock is not provided to the QSPI0 module (the QSPI0 module is disabled)
- 1 = The clock is enabled to the QSPI0 module

6.3.9.13 Reserved—Bit 1

This bit field is reserved. It must be set to 0.

6.3.9.14 PWM Clock Enable (PWM)—Bit 0

- 0 = The clock is not provided to the PWM module (the PWM module is disabled)
- 1 = The clock is enabled to the PWM module

6.3.10 Peripheral Clock Enable Register 1 (SIM_PCE1)

See **Section 6.3.9** for general information about Peripheral Clock Enable registers.

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	PIT0	0	0	0	0	0	0	0	0	TA3	TA2	TA1	TA0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-11 Peripheral Clock Enable Register 1 (SIM_PCE1)

6.3.10.1 Reserved—Bit 15 - 13

This bit field is reserved. Each bit must be set to 0.

6.3.10.2 Programmable Interval Timer 0 Clock Enable (PIT0)—Bit 12

- 0 = The clock is not provided to the PIT0 module (the PIT0 module is disabled)
- 1 = The clock is enabled to the PIT0 module

6.3.10.3 Reserved—Bits 11–4

This bit field is reserved. Each bit must be set to 0.

6.3.10.4 Quad Timer A, Channel 3 Clock Enable (TA3)—Bit 3

- 0 = The clock is not provided to the Timer A3 module (the Timer A3 module is disabled)
- 1 = The clock is enabled to the Timer A3 module

6.3.10.5 Quad Timer A, Channel 2 Clock Enable (TA2)—Bit 2

- 0 = The clock is not provided to the Timer A2 module (the Timer A2 module is disabled)
- 1 = The clock is enabled to the Timer A2 module

6.3.10.6 Quad Timer A, Channel 1 Clock Enable (TA1)—Bit 1

- 0 = The clock is not provided to the Timer A1 module (the Timer A1 module is disabled)
- 1 = The clock is enabled to the Timer A1 module

6.3.10.7 Quad Timer A, Channel 0 Clock Enable (TA0)—Bit 0

- 0 = The clock is not provided to the Timer A0 module (the Timer A0 module is disabled)
- 1 = The clock is enabled to the Timer A0 module

6.3.11 Stop Disable Register 0 (SD0)

By default, peripheral clocks are disabled during Stop mode in order to maximize power savings. This register will allow an individual peripheral to operate in Stop mode. Since asserting an interrupt causes the system to return to Run mode, this feature is provided so that selected peripherals can be left operating in Stop mode for the purpose of generating a wake-up interrupt.

For power-conscious applications, it is recommended that only a minimum set of peripherals be configured to remain operational during Stop mode.

Peripherals should be put in a non-operating (disabled) configuration prior to entering Stop mode unless their corresponding Stop Disable control is set to 1. Refer to the **56F802X and 56F803X Peripheral Reference Manual** for further details. Reads and writes cannot be made to a module that has its clock disabled.

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	CMPB_SD	CMPA_SD	DAC1_SD	DAC0_SD	0	ADC_SD	0	0	0	I2C_SD	0	QSCI0_SD	0	QSPI0_SD	0	PWM_SD
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-12 Stop Disable Register 0 (SD0)

6.3.11.1 Comparator B Clock Stop Disable (CMPB_SD)—Bit 15

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.2 Comparator A Clock Stop Disable (CMPA_SD)—Bit 14

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.3 Digital-to-Analog Converter 0 Clock Stop Disable (DAC1_SD)—Bit 13

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.4 Digital-to-Analog Converter 0 Clock Stop Disable (DAC0_SD)—Bit 12

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.5 Reserved—Bit 11

This bit field is reserved. It must be set to 0.

6.3.11.6 Analog-to-Digital Converter Clock Stop Disable (ADC_SD)—Bit 10

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.7 Reserved—Bits 9–7

This bit field is reserved. Each bit must be set to 0.

6.3.11.8 Inter-Integrated Circuit Clock Stop Disable (I2C_SD)—Bit 6

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.9 Reserved—Bit 5

This bit field is reserved. It must be set to 0.

6.3.11.10 QSCI0 Clock Stop Disable (QSCI0_SD)—Bit 4

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.11 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.11.12 QSPI0 Clock Stop Disable (QSPI0_SD)—Bit 2

Each bit controls clocks to the indicated peripheral.

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.13 Reserved—Bit 1

This bit field is reserved. It must be set to 0.

6.3.11.14 PWM Clock Stop Disable (PWM_SD)—Bit 0

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.12 Stop Disable Register 1 (SD1)

See **Section 6.3.11** for general information about Stop Disable Registers.

Base + $F	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	PIT0_SD	0	0	0	0	0	0	0	0	TA3_SD	TA2_SD	TA1_SD	TA0_SD
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-13 Stop Disable Register 1 (SD1)

6.3.12.1 Reserved—Bit 15-13

This bit field is reserved. Each bit must be set to 0.

6.3.12.2 Programmable Interval Timer 0 Clock Stop Disable (PIT0_SD)—Bit 12

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

6.3.12.3 Reserved—Bits 11–4

This bit field is reserved. Each bit must be set to 0.

6.3.12.4 Quad Timer A, Channel 3 Clock Stop Disable (TA3_SD)—Bit 3

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

6.3.12.5 Quad Timer A, Channel 2 Clock Stop Disable (TA2_SD)—Bit 2

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

6.3.12.6 Quad Timer A, Channel 1 Clock Stop Disable (TA1_SD)—Bit 1

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

6.3.12.7 Quad Timer A, Channel 0 Clock Stop Disable (TA0_SD)—Bit 0

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

6.3.13 I/O Short Address Location Register High (SIM_IOSAHI)

In I/O short address mode, the instruction specifies only 6 LSBs of the effective address; the upper 18 bits are “hard coded” to a specific area of memory. This scheme allows efficient access to a 64-location area in peripheral space with single word instruction. Short address location registers specify the upper 18 bits of I/O address, which are “hard coded”. These registers allow access to peripherals using I/O short address mode, regardless of the physical location of the peripheral, as shown in **Figure 6-14**.

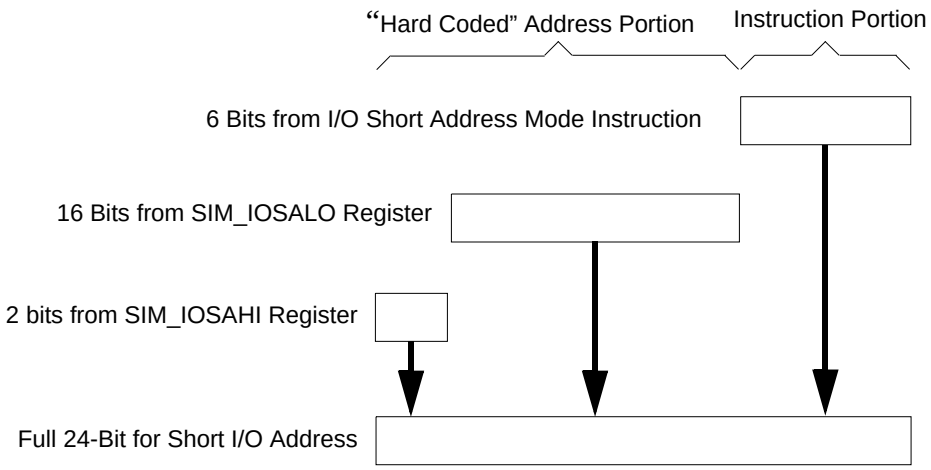


Figure 6-14 I/O Short Address Determination

With this register set, software can set the SIM_IOSAHI and SIM_IOSALO registers to point to its peripheral registers and then use the I/O short addressing mode to access them.

Note: The default value of this register set points to the EOnCE registers.

Note: The pipeline delay between setting this register set and using short I/O addressing with the new value is five instruction cycles.

Base + $10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ISAL[23:22]	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Figure 6-15 I/O Short Address Location High Register (SIM_IOSAHI)

6.3.13.1 Reserved—Bits 15—2

This bit field is reserved. Each bit must be set to 0.

6.3.13.2 Input/Output Short Address Location (ISAL[23:22])—Bits 1–0

This field represents the upper two address bits of the “hard coded” I/O short address.

6.3.14 I/O Short Address Location Register Low (SIM_IOSALO)

See **Section 6.3.13** for general information about I/O short address location registers.

Base + $11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	ISAL[21:6]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-16 I/O Short Address Location Low Register (SIM_IOSALO)

6.3.14.1 Input/Output Short Address Location (ISAL[21:6])—Bits 15–0

This field represents the lower 16 address bits of the “hard coded” I/O short address.

6.3.15 Protection Register (SIM_PROT)

This register provides write protection of selected control fields for safety-critical applications. The primary purpose is to prevent unsafe conditions due to the unintentional modification of these fields between the onset of a code runaway and a reset by the COP watchdog. The GPIO and Internal Peripheral Select Protection (GIPSP) field protects the contents of registers in the SIM and GPIO modules that control inter-peripheral signal muxing and GPIO configuration. The Peripheral Clock Enable Protection (PCEP) field protects the SIM registers’ contents, which contain peripheral clock controls. Some peripherals provide additional safety features. Refer to the **56F802X and 56F803X Peripheral Reference Manual** for details.

Flexibility is provided so that write protection control values may themselves be optionally locked (write-protected). Protection controls in this register have two bit values which determine the setting of the control and whether the value is locked. While a protection control remains unlocked, protection can be disabled and re-enabled by software. Once a protection control is locked, its value can only be altered by a chip reset, which restores its default non-locked value.

Base + $12	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	0	PCEP		GIPSP	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-17 Protection Register (SIM_PROT)

6.3.15.1 Reserved—Bits 15–4

This bit field is reserved. Each bit must be set to 0.

6.3.15.2 Peripheral Clock Enable Protection (PCEP)—Bits 3–2

These bits enable write protection of all fields in the PCE*n*, SD*n*, and PCR registers in the SIM module.

- 00 = Write protection off (default)
- 01 = Write protection on
- 10 = Write protection off and locked until chip reset
- 11 = Write protection on and locked until chip reset

6.3.15.3 GPIO and Internal Peripheral Select Protection (GIPSP)—Bits 1–0

These bits enable write protection of GPS*n* and IPS*n* registers in the SIM module and write protect all GPIO*x*_PEREN, GPIO*x*_PPOUTM and GPIO*x*_DRIVE registers in GPIO modules.

- 00 = Write protection off (default)
- 01 = Write protection on
- 10 = Write protection off and locked until chip reset
- 11 = Write protection on and locked until chip reset

Note: The PWM fields in the CLKOUT register are also write protected by GIPSP. They are reserved for in-house test only.

6.3.16 SIM GPIO Peripheral Select Register 0 for GPIOA (SIM_GPSA0)

Most I/O pins have an associated GPIO function. In addition to the GPIO function, I/O can be configured to be one of several peripheral functions. The GPIO*x*_PEREN register within the GPIO module controls the selection between peripheral or GPIO control of the I/O pins. The GPIO function is selected when the GPIO*x*_PEREN bit for the I/O is 0. When the GPIO*x*_PEREN bit of the GPIO is 1, the fields in the GPS*n* registers select which peripheral function has control of the I/O. **Figure 6-18** illustrates the output path to an I/O pin when an I/O has two peripheral functions. Similar muxing is required on peripheral function inputs to receive input from the properly selected I/O pin.

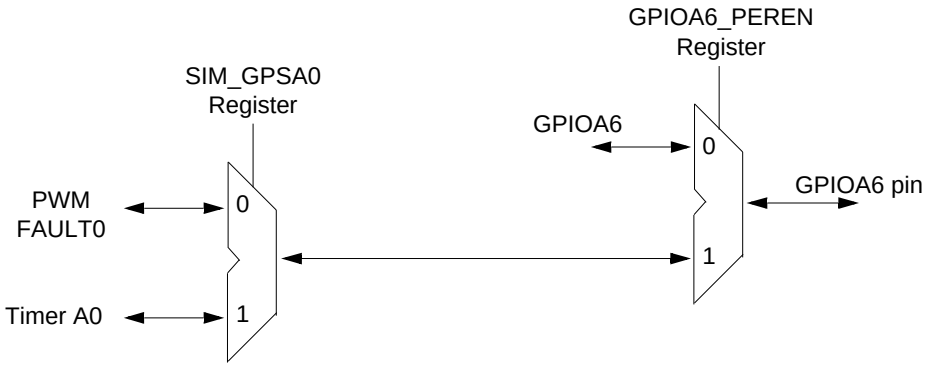


Figure 6-18 Overall Control of Signal Source Using SIM_GPS*nn* Control

In some cases, the user can choose peripheral function between several I/O, each of which have the option to be programmed to control a specific peripheral function. If the user wishes to use that function, only one of these I/O must be configured to control that peripheral function. If more than one I/O is configured to control the peripheral function, the peripheral output signal will fan out to each I/O, but the peripheral input signal will be the logical OR and AND of all the I/O signals.

Complete lists of I/O muxings are provided in **Table 2-3**.

The GPS*n* setting can be altered during normal operation, but a delay must be inserted between the time when one function is disabled and another function is enabled.

Note: After reset, all I/O pins are GPIO, except the JTAG pins and the $\overline{\text{RESET}}$ pin.

Base + $13	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	GPS_A6	GPS_A5		GPS_A4		0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-19 GPIO Peripheral Select Register 0 for GPIOA (SIM_GPSA0)

6.3.16.1 Reserved—Bits 15–13

This bit field is reserved. Each bit must be set to 0.

6.3.16.2 Configure GPIOA6 (GPS_A6)—Bit 12

This field selects the alternate function for GPIOA6.

- 0 = FAULT0 - PWM FAULT0 Input (default)
- 1 = TA0 - Timer A0

6.3.16.3 Configure GPIOA5 (GPS_A5)—Bits 11–10

This field selects the alternate function for GPIOA5.

- 00 = PWM5 - PWM5 (default)
- 01 = FAULT2 - PWM FAULT2 Input
- 10 = TA3 - Timer A3
- 11 = Reserved

6.3.16.4 Configure GPIOA4 (GPS_A4)—Bits 9–8

This field selects the alternate function for GPIOA4.

- 00 = PWM4 - PWM4 (default)
- 01 = FAULT1 - PWM FAULT1 Input
- 10 = TA2 - Timer A2
- 11 = Reserved

6.3.16.5 Reserved—Bits 7–0

This bit field is reserved. Each bit must be set to 0.

6.3.17 SIM GPIO Peripheral Select Register 0 for GPIOB (SIM_GPSB0)

See **Section 6.3.16** for general information about GPIO Peripheral Select Registers.

Base + $15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	GPS_B6		GPS_B5		GPS_B4			GPS_B3		GPS_B2		0	GPS_B1	0	GPS_B0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-20 GPIO Peripheral Select Register 0 for GPIOB (SIM_GPSB0)

6.3.17.1 Reserved—Bit 15

This bit field is reserved. It must be set to 0.

6.3.17.2 Configure GPIOB6 (GPS_B6)—Bits 14–13

This field selects the alternate function for GPIOB6.

- 00 = RXD0 - QSCI0 Receive Data (default)
- 01 = SDA - I2C Serial Data
- 10 = CLKIN - External Clock Input
- 11 = Reserved

6.3.17.3 Configure GPIOB5 (GPS_B5)—Bits 12–11

This field selects the alternate function for GPIOB5.

- 00 = TA1 - Timer A1 (default)
- 01 = FAULT3 - PWM FAULT3 Input
- 10 = CLKIN - External Clock Input
- 11 = Reserved

6.3.17.4 Configure GPIOB4 (GPS_B4)—Bits 10–8

This field selects the alternate function for GPIOB4.

- 000 = TA0 - Timer A0 (default)
- 001 = CLKO - Clock Output
- 010 = Reserved
- 011 = TB0 - Timer B0
- 100 = PSRC2 - PWM4 / PWM5 Pair External Source
- 11x = Reserved
- 1x1 = Reserved

6.3.17.5 Configure GPIOB3 (GPS_B3)—Bits 7–6

This field selects the alternate function for GPIOB3.

- 00 = MOSI0 - QSPI0 Master Out/Slave In (default)
- 01 = TA3 - Timer A3
- 10 = PSRC1 - PWM2 / PWM3 Pair External Source
- 11 = Reserved

6.3.17.6 Configure GPIOB2 (GPS_B2)—Bits 5–4

This field selects the alternate function for GPIOB2.

- 00 = MISO0 QSPI0 Master In/Slave Out (default)
- 01 = TA2 - Timer A2
- 10 = PSRC0 - PWM0 / PWM1 Pair External Source
- 11 = Reserved

6.3.17.7 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.17.8 Configure GPIOB1 (GPS_B1)—Bit 2

This field selects the alternate function for GPIOB1.

- 0 = $\overline{SS}$0 - QSPI0 Slave Select (default)
- 1 = SDA - I2C Serial Data

6.3.17.9 Reserved—Bit 1

This bit field is reserved. It must be set to 0.

6.3.17.10 Configure GPIOB0 (GPS_B0)—Bits 0

This field selects the alternate function for GPIOB0.

- 0 = SCLK0 - QSPI0 Serial Clock (default)
- 1 = SCL - I^2C Serial Clock

6.3.18 SIM GPIO Peripheral Select Register 1 for GPIOB (SIM_GPSB1)

See **Section 6.3.16** for general information about GPIO Peripheral Select Registers.

Base + $16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPS_B7
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-21 GPIO Peripheral Select Register 1 for GPIOB (SIM_GPSB1)

6.3.18.1 Reserved—Bits 15–1

This bit field is reserved. Each bit must be set to 0.

6.3.18.2 Configure GPIOB7 (GPS_B7)—Bit 0

This field selects the alternate function for GPIOB7.

- 0 = TXD0 - QSCI0 Transmit Data (default)
- 1 = SCL - I^2C Serial Clock

6.3.19 Internal Peripheral Source Select Register 0 for Pulse Width Modulator (SIM_IPS0)

The internal integration of peripherals provides input signal source selection for peripherals where an input signal to a peripheral can be fed from one of several sources. These registers are organized by peripheral type and provide a selection list for every peripheral input signal that has more than one alternative source to indicate which source is selected.

If one of the alternative sources is GPIO, the setting in these registers must be made consistently with the settings in the GPS*n* and GPIO*x*_PEREN registers. Specifically, when an IPS*n* field is configured to select an I/O pin as the source, then GPS*n* register settings must configure only one I/O pin to feed this peripheral input function. Also, the GPIO*x*_PEREN bit for that I/O pin must be set to 1 to enable peripheral control of the I/O.

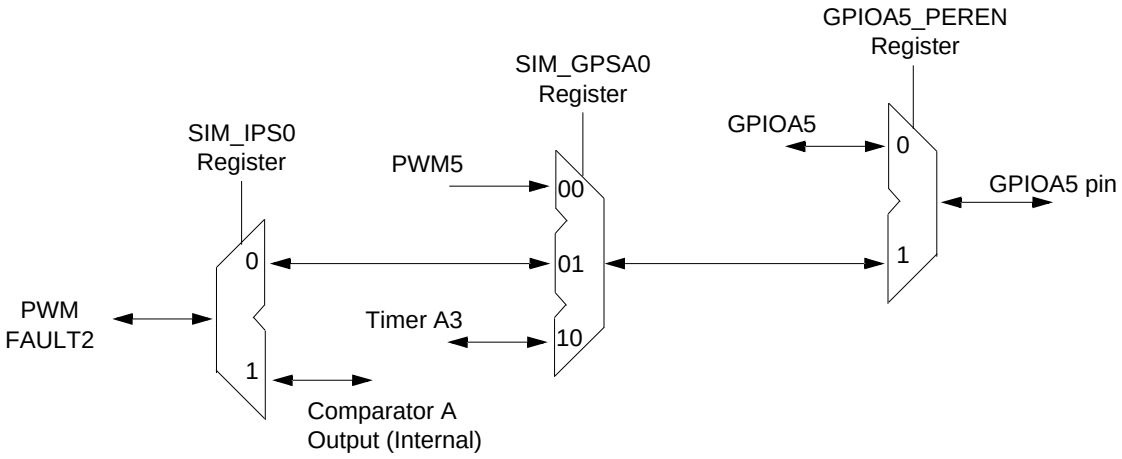


Figure 6-22 Overall Control of Signal Source using SIM_IPS*n* Control

IPS*n* settings should not be altered while an affected peripheral is in an enabled (operational) configuration. See the **56F802X and 56F803X Peripheral Reference Manual** for details.

Base + $18	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	IPS0_ FAULT2	0	IPS0_ FAULT1	0	0	IPS0_PSRC2			IPS0_PSRC1			IPS0_PSRC0		
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-23 Internal Peripheral Source Select Register for PWM (SIM_IPS0)

6.3.19.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

6.3.19.2 Select Peripheral Input Source for FAULT2 (IPS0_FAULT2)—Bit 13

This field selects the alternate input source signal to feed PWM input FAULT2.

- 0 = I/O Pin (External) - Use PWM FAULT2 Input Pin (default)
- 1 = CMPBO (Internal) - Use Comparator B Output

6.3.19.3 Reserved—Bit 12

This bit field is reserved. It must be set to 0.

6.3.19.4 Select Peripheral Input Source for FAULT1 (IPS0_FAULT1)—Bit 11

This field selects the alternate input source signal to feed PWM input FAULT1.

- 0 = I/O pin (External) - Use PWM FAULT2 Input Pin (default)
- 1 = CMPAO (Internal) - Use Comparator A Output

6.3.19.5 Reserved—Bits 10–9

This bit field is reserved. Each bit must be set to 0.

6.3.19.6 Select Peripheral Input Source for PWM4/PWM5 Pair Source (IPS0_PSRC2)—Bits 8–6

This field selects the alternate input source signal to feed PWM input PSRC2 as the PWM4/PWM5 pair source.

- 000 = Reserved (default)
- 001 = TA3 (Internal) - Use Timer A3 output as PWM source
- 010 = ADC SAMPLE2 (Internal) - Use ADC SAMPLE2 result as PWM source
  - If the ADC conversion result in SAMPLE2 is greater than the value programmed into the High Limit register HLMT2, then PWM4 is set to 0 and PWM5 is set to 1
  - If the ADC conversion result in SAMPLE2 is less than the value programmed into the Low Limit register LLMT2, then PWM4 is set to 1 and PWM5 is set to 0
- 011 = CMPAO (Internal) - Use Comparator A output as PWM source
- 100 = CMPBO (Internal) - Use Comparator B output as PWM source
- 11x = Reserved
- 1x1 = Reserved

6.3.19.7 Select Peripheral Input Source for PWM2/PWM3 Pair Source (IPS0_PSRC1)—Bits 5–3

This field selects the alternate input source signal to feed PWM input PSRC1 as the PWM2/PWM3 pair source.

- 000 = I/O pin (External) - Use a PSRC1 input pin as PWM source (default)
- 001 = TA2 (Internal) - Use Timer A2 output as PWM source
- 010 = ADC SAMPLE1 (Internal) - Use ADC SAMPLE1 result as PWM source
  - If the ADC conversion result in SAMPLE1 is greater than the value programmed into the High Limit register HLMT1, then PWM2 is set to 0 and PWM3 is set to 1
  - If the ADC conversion result in SAMPLE1 is less than the value programmed into the Low Limit register LLMT2, then PWM2 is set to 1 and PWM3 is set to 0
- 011 = CMPAO (Internal) - Use Comparator A output as PWM source
- 100 = CMPBO (Internal) - Use Comparator B output as PWM source
- 11x = Reserved
- 1x1 = Reserved

6.3.19.8 Select Peripheral Input Source for PWM0/PWM1 Pair Source (IPS0_PSRC0)—Bits 2–0

This field selects the alternate input source signal to feed PWM input PSRC0 as the PWM0/PWM1 pair source.

- 000 = I/O pin (External) - Use a PSRC0 input pin as PWM source (default)
- 001 = TA0 (Internal) - Use Timer A0 output as PWM source
- 010 = ADC SAMPLE0 (Internal) - Use ADC SAMPLE0 result as PWM source
  - — If the ADC conversion result in SAMPLE0 is greater than the value programmed into the High Limit register HLMT1, then PWM0 is set to 0 and PWM1 is set to 1
  - — If the ADC conversion result in SAMPLE0 is less than the value programmed into the Low Limit register LLMT2, then PWM0 is set to 1 and PWM1 is set to 0
- 011 = CMPAO (Internal) - Use Comparator A output as PWM source
- 100 = CMPBO (Internal) - Use Comparator B output as PWM source
- 11x = Reserved
- 1x1 = Reserved

6.3.20 Internal Peripheral Source Select Register 1 for Digital-to-Analog Converters (SIM_IPS1)

See **Section 6.3.19** for general information about Internal Peripheral Source Select registers.

Base + $19	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	IPS1_DSYNC1			0	IPS1_DSYNC0		
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-24 Internal Peripheral Source Select Register for DACs (SIM_IPS1)

6.3.20.1 Reserved—Bits 15–7

This bit field is reserved. Each bit must be set to 0.

6.3.20.2 Select Peripheral Input Source for SYNC Input to DAC 1 (ISS1_DSYNC1)-Bits 6-4

This field selects the alternate input source signal to feed DAC1 SYNC input.

- 000 = PIT0 (Internal) — Use Programmable Interval Timer 0 Output as DAC SYNC input (default)
- 001 = Reserved
- 010 = Reserved
- 011 = PWM SYNC (Internal) - Use PWM reload synchronization signal as DAC SYNC input
- 100 = TA0 (Internal) - Use Timer A0 output as DAC SYNC input
- 101 = TA1 (Internal) - Use Timer A1 output as DAC SYNC input
- 11x = Reserved

6.3.20.3 Select Peripheral Input Source for SYNC Input to DAC 0 (ISS1_DSYNC0)—Bits 2–0

This field selects the alternate input source signal to feed DAC0 SYNC input.

- 000 = PIT0 (Internal) - Use Programmable Interval Timer 0 Output as DAC SYNC input (default)
- 001 = Reserved
- 010 = Reserved
- 011 = PWM SYNC (Internal) - Use PWM reload synchronization signal as DAC SYNC input
- 100 = TA0 (Internal) - Use Timer A0 output as DAC SYNC input
- 101 = TA1 (Internal) - Use Timer A1 output as DAC SYNC input
- 11x = Reserved

6.3.21 Internal Peripheral Source Select Register 2 for Quad Timer A (SIM_IPS2)

See **Section 6.3.19** for general information about Internal Peripheral Source Select registers.

Base + $1A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	IPS2_ TA3	0	0	0	IPS2_ TA2	0	0	0	IPS2_ TA1	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-25 Internal Peripheral Source Select Register for TMRA (SIM_IPS2)

6.3.21.1 Reserved—Bits 15–13

This bit field is reserved. Each bit must be set to 0.

6.3.21.2 Select Peripheral Input Source for TA3 (IPS2_TA3)—Bit 12

This field selects the alternate input source signal to feed Quad Timer A, input 3.

- 0 = I/O pin (External) - Use Timer A3 input/output pin
- 1 = PWM SYNC (Internal) - Use PWM reload synchronization signal

6.3.21.3 Reserved—Bits 11–9

This bit field is reserved. Each bit must be set to 0.

6.3.21.4 Select Input Source for TA2 (ISS2_TA2)—Bit 8

This field selects the alternate input source signal to feed Quad Timer A, input 2.

- 0 = I/O pin (External) - Use Timer A2 input/output pin
- 1 = CMPBO (Internal) - Use Comparator B output

6.3.21.5 Reserved—Bits 7–5

This bit field is reserved. Each bit must be set to 0.

6.3.21.6 Select Peripheral Input Source for TA1 (IPS2_TA1)—Bit 4

This field selects the alternate input source signal to feed Quad Timer A, input 1.

- 0 = I/O pin (External) - Use Timer A1 input/output pin
- 1 = CMPAO (Internal) - Use Comparator A output

6.3.21.7 Reserved—Bits 3–0

This bit field is reserved. Each bit must be set to 0.

For Timer A to detect the PWM SYNC signal, the clock rate of both the PWM module and Timer A module must be identical, at either the system clock rate or 3X system clock rate.

6.4 Clock Generation Overview

The SIM uses the master clock (2X system clock) at a maximum of 64MHz from the OCCS module to produce a system clock at a maximum of 32MHz for the peripheral, core, and memory. It divides the master clock by two and gates it with appropriate power mode and clock gating controls. A 3X system high-speed peripheral clock input from OCCS operates at three times the system clock at a maximum of 96MHz and can be an optional clock for PWM, Timer A, and I^2C modules. These clocks are generated by gating the 3X system high-speed peripheral clock with appropriate power mode and clock gating controls.

The OCCS configuration controls the operating frequency of the SIM's master clocks. In the OCCS, either an external clock (CLKIN), a crystal oscillator, or the relaxation oscillator can be selected as the master clock source (MSTR_OSC). An external clock can be operated at any frequency up to 64MHz. The crystal oscillator can be operated only at a maximum of 8MHz. The relaxation oscillator can be operated at full speed (8MHz), standby speed (200kHz using ROSB), or powered down (using ROPD). An 8MHz MSTR_OSC can be multiplied to 196MHz using the PLL and postscaled to provide a variety of high-speed clock rates. Either the postscaled PLL output or MSTR_OSC signal can be selected to produce the master clocks to the SIM. When the PLL is selected, both the 3X system clock and the 2X system clock are enabled. If the PLL is not selected, the 3X system clock is disabled and the master clock is MSTR_OSC.

In combination with the OCCS module, the SIM provides power modes (see **Section 6.5**), clock enables, and clock rate controls to provide flexible control of clocking and power utilization. The clock rate controls enable the high-speed clocking option for the two quad timers (TMRA and TMRB) and PWM, but requires the PLL to be on and selected. Refer to the **56F802X and 56F803X Peripheral Reference Manual** for further details. The peripheral clock enable controls can be used to disable an individual peripheral clock when it is not used.

6.5 Power-Saving Modes

The 56F8023 operates in one of five Power-Saving modes, as shown in **Table 6-2**.

Table 6-2 Clock Operation in Power-Saving Modes

Mode	Core Clocks	Peripheral Clocks	Description
Run	Core and memory clocks enabled	Peripheral clocks enabled	Device is fully functional
Wait	Core and memory clocks disabled	Peripheral clocks enabled	Core executes WAIT instruction to enter this mode. Typically used for power-conscious applications. Possible recoveries from Wait mode to Run mode are: 1. Any interrupt 2. Executing a Debug mode entry command during the 56800E core JTAG interface 3. Any reset (POR, external, software, COP)
Stop	Master clock generation in the OCCS remains operational, but the SIM disables the generation of system and peripheral clocks.		Core executes STOP instruction to enter this mode. Possible recoveries from Stop mode to Run mode are: 1. Interrupt from any peripheral configured in the CTRL register to operate in Stop mode (TA0-3, QSCI0, PIT0-1, CAN, CMPA-B) 2. Low-voltage interrupt 3. Executing a Debug mode entry command using the 56800E core JTAG interface 4. Any reset (POR, external, software, COP)
Standby	The OCCS generates the master clock at a reduced frequency (400kHz). The PLL is disabled and the high-speed peripheral option is not available. System and peripheral clocks operate at 200kHz.		The user configures the OCCS and SIM to select the relaxation oscillator clock source (PRECS), shut down the PLL (PLLPD), put the relaxation oscillator in Standby mode (ROSB), and put the large regulator in Standby (LRSTDBY). The device is fully operational, but operating at a minimum frequency and power configuration. Recovery requires reversing the sequence used to enter this mode (allowing for PLL lock time).
Power-Down	Master clock generation in the OCCS is completely shut down. All system and peripheral clocks are disabled.		The user configures the OCCS and SIM to enter Standby mode as shown in the previous description, followed by powering down the oscillator (ROPD). The only possible recoveries from this mode are: 1. External Reset 2. Power-On Reset

The power-saving modes provide additional power management options by disabling the clock, reconfiguring the voltage regulator clock generation to manage power utilization, as shown in **Table 6-2**. Run, Wait, and Stop modes provide methods of enabling/disabling the peripheral and/or core clocking as a group. Stop disable controls for an individual peripheral are provided in the SD*n* registers to override the default behavior of Stop mode. By asserting a peripheral's Stop disable bit, the peripheral clock continues

to operate in Stop mode. This is useful to generate interrupts which will recover the device from Stop mode to Run mode. Standby mode provides normal operation but at very low speed and power utilization. It is possible to invoke Stop or Wait mode while in Standby mode for even greater levels of power reduction. A 400kHz external clock can optionally be used in Standby mode to produce the required Standby 200kHz system clock rate. Power-down mode, which selects the ROSC clock source but shuts it off, fully disables the device and minimizes its power utilization but is only recoverable via reset.

When the PLL is not selected and the system bus is operating at 200kHz or less, the large regulator can be put into its Standby mode (LRSTDBY) to reduce the power utilization of that regulator.

All peripherals, except the COP/watchdog timer, run at the system clock frequency or optional 3X system clock for PWM, Timers, and I^2C. The COP timer runs at OSC_CLK / 1024. The maximum frequency of operation is 32MHz.

6.6 Resets

The SIM supports five sources of reset, as shown in **Figure 6-26**. The two asynchronous sources are the external reset pin and the Power-On Reset (POR). The three synchronous sources are the software reset (SW reset), which is generated within the SIM itself by writing the SIM_CTRL register in **Section 6.3.1**, the COP time-out reset (COP_TOR), and the COP loss-of-reference reset (COP_LOR). The reset generation module has three reset detectors, which resolve into four primary resets. These are outlined in **Table 6-3**. The JTAG circuitry is reset by the Power-On Reset.

Table 6-3 Primary System Resets

	Reset Sources				
Reset Signal	**POR**	**External**	**Software**	**COP**	**Comments**
EXTENDED_$\overline{\text{POR}}$	X				Stretched version of $\overline{\text{POR}}$ released 64 OSC_CLK cycles after $\overline{\text{POR}}$ deasserts
CLKGEN_$\overline{\text{RST}}$	X	X	X	X	Released 32 OSC_CLK cycles after all reset sources, including EXTENDED_$\overline{\text{POR}}$, have released
PERIP_$\overline{\text{RST}}$	X	X	X	X	Releases 32 SYS_CLK cycles after the CLKGEN_$\overline{\text{RST}}$ is released
CORE_$\overline{\text{RST}}$	X	X	X	X	Releases 32 SYS_CLK cycles after PERIP_$\overline{\text{RST}}$ is released

Figure 6-26 provides a graphic illustration of the details in **Table 6-3**. Note that the POR_Delay blocks use the OSC_CLK as their time base, since other system clocks are inactive during this phase of reset.

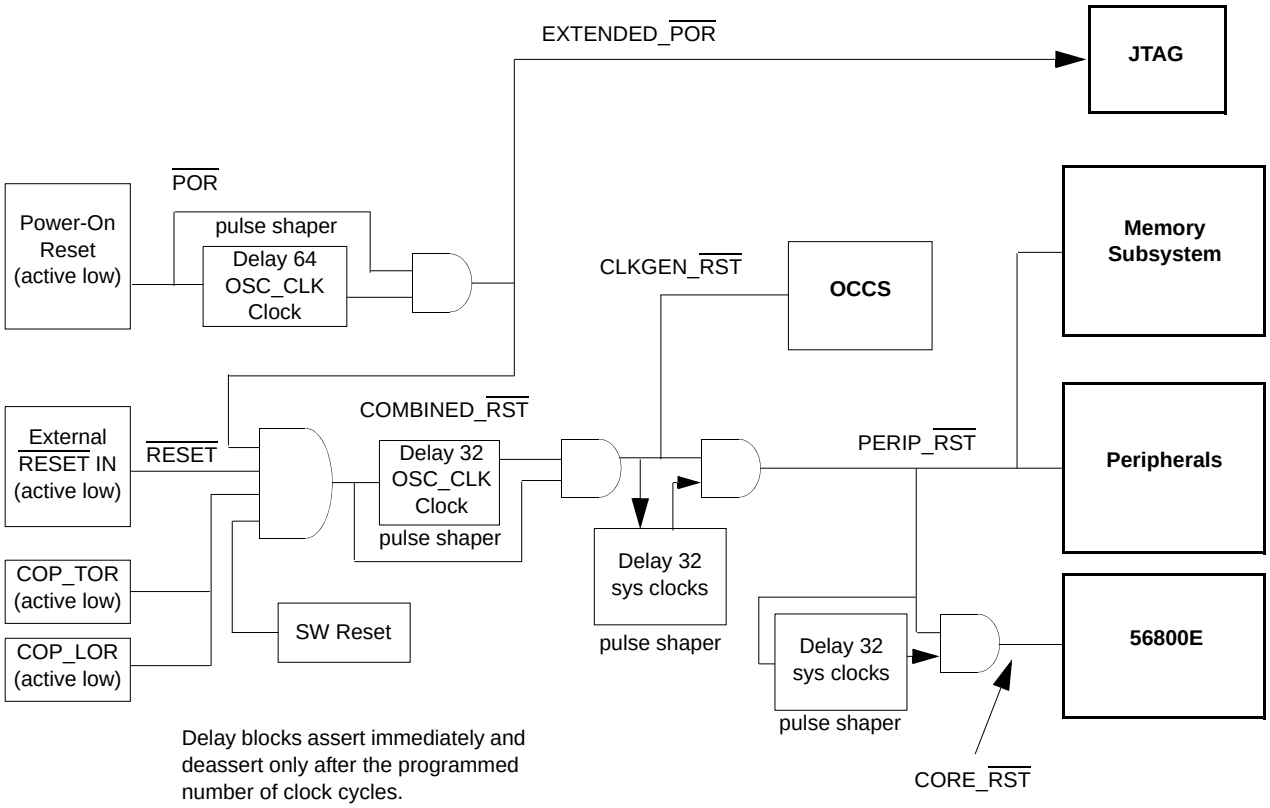


Figure 6-26 Sources of RESET Functional Diagram (Test modes not included)

POR resets are extended 64 OSC_CLK clocks to stabilize the power supply and clock source. All resets are subsequently extended for an additional 32 OSC_CLK clocks and 64 system clocks as the various internal reset controls are released. Given the normal relaxation oscillator rate of 8MHz, the duration of a POR reset from when power comes on to when code is running is 28µS. An external reset generation circuit may also be used. A description of how these resets are used to initialize the clocking system and system modules is included in **Section 6.7**.

6.7 Clocks

The memory, peripheral and core clocks all operate at the same frequency (32MHz maximum), with the exception of the peripheral clocks for quad timers TMRA and TMRB and the PWM, which have the option to operate at 3X system clock. The SIM is responsible for clock distributions.

While the SIM generates the ADC peripheral clock in the same way it generates all other peripheral clocks, the ADC standby and conversion clocks are generated by a direct interface between the ADC and the OCCS module.

The deassertion sequence of internal resets coordinates the device start up, including the clocking system start up. The sequence is described in the following steps:

1. As power is applied, the Relaxation Oscillator starts to operate. When a valid operating voltage is reached, the POR reset will release.
2. The release of POR reset permits operation of the POR reset extender. The POR extender generates an extended POR reset, which is released 64 OSC_CLK cycles after POR reset. This provides an additional time period for the clock source and power to stabilize.
3. A Combined reset consists of the OR of the extended POR reset, the external reset, the COP reset and Software reset. The entire device, except for the POR extender, is held reset as long as Combined reset is asserted. The release of Combined reset permits operation of the CTRL register, the Synchronous reset generator, and the CLKGEN reset extender.
4. The Synchronous reset generator generates a reset to the Software and COP reset logic. The COP and Software reset logic is released three OSC_CLK cycles after Combined reset deasserts. This provides a reasonable minimum duration to the reset for these specialized functions.
5. The CLKGEN reset extender generates the CLKGEN reset used by the clock generation logic. The CLKGEN reset is released 32 OSC_CLK cycles after Combined reset deasserts. This provides a window in which the SIM stabilizes the master clock inputs to the clock generator.
6. The release of CLKGEN reset permits operation of the clock generation logic and the Peripheral reset extender. The Peripheral reset extender generates the Peripheral reset, which is released 32 SYS_CLK cycles after CLKGEN reset. This provides a window in which peripheral and core logic remain clocked, but in reset, so that synchronous resets can be resolved.
7. The release of Peripheral reset permits operation of the peripheral logic and the Core reset extender. The Core reset extender generates the Core reset, which is released 32 SYS_CLK cycles after the Peripheral reset. This provides a window in which critical peripheral start-up functions, such as Flash Security in the Flash memory, can be implemented.
8. The release of Core reset permits execution of code by the 56800E core and marks the end of the system start-up sequence.

Figure 6-27 illustrates clock relationships to one another and to the various resets as the device comes out of reset. $\overline{\text{RST}}$ is assumed to be the logical AND of all active-low system resets (for example, POR, external reset, COP and Software reset). In the 56F8023, this signal will be stretched by the SIM for a period of time (up to 96 OSC_CLK clock cycles, depending upon the status of the POR) to create the clock generation reset signal (CLKGEN_$\overline{\text{RST}}$). The SIM should deassert CLKGEN_$\overline{\text{RST}}$ synchronously with the negative edge of OSC_CLK in order to avoid skew problems. CLKGEN_$\overline{\text{RST}}$ is delayed 32 SYS_CLK cycles to create the peripheral reset signal (PERIP_$\overline{\text{RST}}$). PERIP_$\overline{\text{RST}}$ is then delayed by 32 SYS_CLK cycles to create CORE_$\overline{\text{RST}}$. Both PERIP_$\overline{\text{RST}}$ and CORE_$\overline{\text{RST}}$ should be released on the negative edge of SYS_CLK_D as shown. This phased releasing of system resets is necessary to give some peripherals (for example, the Flash interface unit) set-up time prior to the 56800E core becoming active.

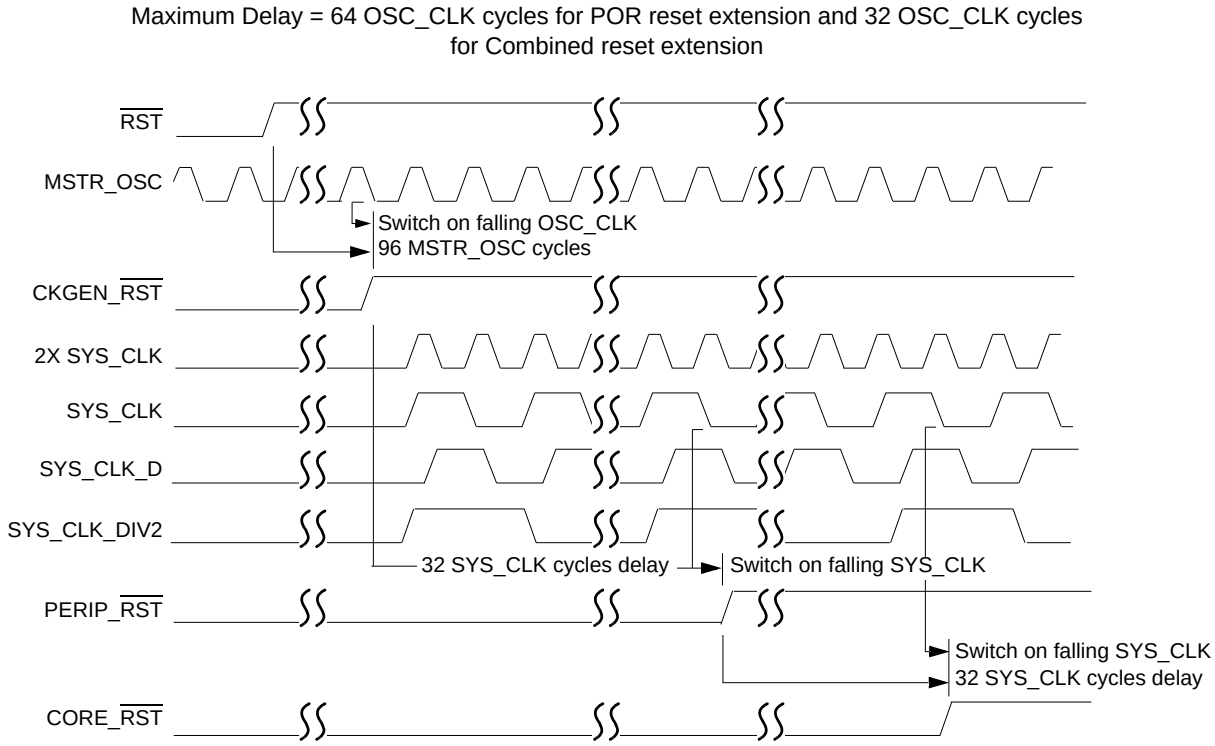


Figure 6-27 Timing Relationships of Reset Signal to Clocks

6.8 Interrupts

The SIM generates no interrupts.

Part 7 Security Features

The 56F8023 offers security features intended to prevent unauthorized users from reading the contents of the flash memory (FM) array. The 56F8023's flash security consists of several hardware interlocks that prevent unauthorized users from gaining access to the flash array.

After flash security is set, an authorized user is still able to access on-chip memory if a user-defined software subroutine, which reads and transfers the contents of internal memory via serial communication peripherals, is included in the application software.

7.1 Operation with Security Enabled

After the user has programmed flash with the application code, the 56F8023 can be secured by programming the security word $0002 into program memory location $00 7FF7. This non-volatile word will keep the device secured through reset and through power-down of the device. Refer to the flash memory chapter in the **56F802x and 56F803x Peripheral Reference Manual** for the details. When flash security mode is enabled, the 56F8023 will disable the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Lock and Unlock Mechanisms

There are several methods that effectively lock or unlock the on-chip flash.

7.2.1 Disabling EOnCE Access

On-chip flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E CPU. The TCK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register, but proper implementation of flash security will block any attempt to access the internal flash memory via the EOnCE port when security is enabled.

7.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared). This does not compromise security, as the entire contents of the user's secured code stored in flash are erased before security is disabled on the device on the next reset or power-up sequence.

To start the lockout recovery sequence via JTAG, the JTAG public instruction (LOCKOUT_RECOVERY) must first be shifted into the chip-level TAP controller's instruction register. Once the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, the user must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the **56F802x and 56F803x Peripheral Reference Manual** for more details, or contact Freescale.

Note: Once the lockout recovery sequence has completed, the user must reset both the JTAG-TAP controller and device to return to normal unsecured operation. Power-on reset will reset both too.

7.2.3 Flash Lockout Recovery using CodeWarrior

CodeWarrior can unlock a device by selecting the *Debug* menu, then selecting *DSP56800E*, followed by *Unlock Flash*. Another mechanism is also built into CodeWarrior using the device's memory configuration file. The command "*Unlock_Flash_on_Connect 1*" in the *.cfg* file accomplishes the same task as using the *Debug* menu.

This lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared).

7.2.4 Flash Lockout Recovery without mass erase

A user can un-secure a secured device by programming the word $0000 into program memory location $00 7FF7. After completing the programming, both the JTAG TAP controller and the device must be reset in order to return to normal unsecured operation. Power-on reset will also reset both.

The user is responsible for directing the device to invoke the flash programming subroutine to reprogram the word $0000 into program memory location $00 7FF7. This is done by, for example, toggling a specific

pin or downloading a user-defined key through serial interfaces.

Note: Flash contents can only be programmed for 1s to 0s.

7.3 Product Analysis

The recommended method of unsecuring a secured device for product analysis of field failures is via the method described in section 7.2.4. The customer would need to supply Technical Support with the details of the protocol to access the subroutines in flash memory. An alternative method for performing analysis on a secured device would be to mass-erase and reprogram the flash with the original code, but modify the security word or not program the security word.

Part 8 General-Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F802X and 56F803X Peripheral Reference Manual** and contains only chip-specific information. This information supersedes the generic information in the **56F802X and 56F803X Peripheral Reference Manual**.

8.2 Configuration

There are four GPIO ports defined on the 56F8023. The width of each port, the associated peripheral and reset functions are shown in **Table 8-1**. The specific mapping of GPIO port pins is shown in **Table 8-2**. Additional details are shown in **Tables 2-2** and **2-3**.

Table 8-1 GPIO Ports Configuration

GPIO Port	Available Pins in 56F8023	Peripheral Function	Reset Function
A	8	PWM, Timer, QSPI, Comparator, Reset	GPIO, $\overline{\text{RESET}}$
B	8	QSPI, I^2C, PWM, Clock, Comparator, Timer	GPIO
C	6	ADC, Comparator, QSCI	GPIO
D	4	Clock, Oscillator, JTAG	GPIO, JTAG

Table 8-2 GPIO External Signals Map

GPIO Function	Peripheral Function	LQFP Package Pin	Notes
GPIOA0	PWM0	29	Defaults to A0
GPIOA1	PWM1	28	Defaults to A1
GPIOA2	PWM2	23	Defaults to A2
GPIOA3	PWM3	24	Defaults to A3
GPIOA4	PWM4 / TA2 / FAULT1	22	SIM register SIM_GPS is used to select between PWM4, TA2, and FAULT1. Defaults to A4
GPIOA5	PWM5 / TA3 / FAULT2	20	SIM register SIM_GPS is used to select between PWM5, TA3, and FAULT2. Defaults to A5
GPIOA6	FAULT0 / TA0	18	SIM register SIM_GPS is used to select between FAULT0 and TA0. Defaults to A6
GPIOA7	$\overline{\text{RESET}}$	15	Defaults to $\overline{\text{RESET}}$
GPIOB0	SCLK0 / SCL	21	SIM register SIM_GPS is used to select between SCLK and SCL. Defaults to B0
GPIOB1	$\overline{\text{SS0}}$ / SDA	2	SIM register SIM_GPS is used to select between $\overline{\text{SS0}}$ and SDA. Defaults to B1
GPIOB2	MISO0 / TA2 / PSRC0	17	SIM register SIM_GPS is used to select between MISO0, TA2, and PSRC0. Defaults to B2
GPIOB3	MOSI0 / TA3 / PSRC1	16	SIM register SIM_GPS is used to select between MOSI0, TA3 and PSRC1. Defaults to B3
GPIOB4	TA0 / CLKO / PSRC2	38	SIM register SIM_GPS is used to select between TA0, CLKO, and PSRC2. Defaults to B4

Table 8-2 GPIO External Signals Map (Continued)

GPIO Function	Peripheral Function	LQFP Package Pin	Notes
GPIOB5	TA1 / FAULT3 / CLKIN	4	SIM register SIM_GPS is used to select between TA1, FAULT3, and CLKIN. CLKIN functionality is enabled using the PLL Control Register within the OCCS block. Defaults to B5
GPIOB6	RXD0 / SDA / CLKIN	1	SIM register SIM_GPS is used to select between RXD0, SDA, and CLKIN. CLKIN functionality is enabled using the PLL Control Register within the OCCS block. Defaults to B6
GPIOB7	TXD0 / SCL	3	SIM register SIM_GPS is used to select between TXD0 and SCL. Defaults to B7
GPIOC0	ANA0 & CMPAI3	12	Defaults to C0
GPIOC1	ANA1	11	Defaults to C1
GPIOC2	ANA2 / V_{REFHA}	10	SIM register SIM_GPS is used to select between ANA2 and V_{REFHA}. Defaults to C2
GPIOC4	ANB0 / CMPBI3	5	SIM register SIM_GPS is used to select between ANB0 and CMPBI3. Defaults to C4
GPIOC5	ANB1	6	Defaults to C5
GPIOC6	ANB2 / V_{REFHB}	7	SIM register SIM_GPS is used to select between ANB2 and V_{REFHB}. Defaults to C6
GPIOD0	TDI	30	Defaults to TDI
GPIOD1	TDO	32	Defaults to TDO
GPIOD2	TCK	14	Defaults to TCK
GPIOD3	TMS	31	Defaults to TMS

8.3 Reset Values

Tables **8-1** and **8-2** detail registers for the 56F8023; Figures **8-1** through **8-4** summarize register maps and reset values.

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOA_PUPEN	R									PU[15:0]							
		W																
		RS	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$1	GPIOA_DATA	R									D[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOA_DDIR	R									DD[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOA_PEREN	R									PE[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$4	GPIOA_IASSRT	R									IA[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOA_IEN	R									IEN[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOA_IEPOL	R									IEPOL[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOA_IPEND	R									IPR[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOA_IEDGE	R									IES[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOA_PPOUTM	R									OEN[15:0]							
		W																
		RS	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$A	GPIOA_RDATA	R									RAW DATA[15:0]							
		W																
		RS	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOA_DRIVE	R									DRIVE[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-1 GPIOA Register Map Summary

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOB_PUPEN	R									PU[15:0]							
		W																
		RS	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$1	GPIOB_DATA	R									D[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOB_DDIR	R									DD[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOB_PEREN	R									PE[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$4	GPIOB_IASSRT	R									IA[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOB_IEN	R									IEN[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOB_IEPOL	R									IEPOL[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOB_IPEND	R									IPR[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOB_IEDGE	R									IES[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOB_PPOUTM	R									OEN[15:0]							
		W																
		RS	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$A	GPIOB_RDATA	R	0	0							RAW DATA[15:0]							
		W																
		RS	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOB_DRIVE	R									DRIVE[15:0]							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-2 GPIOB Register Map Summary

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOC_PUPEN	R										PU[15:0]				PU		
		W																
		RS	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$1	GPIOC_DATA	R										D[15:0]				D		
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOC_DDIR	R										DD[15:0]				DD		
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOC_PEREN	R										PE[15:0]				PE		
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$4	GPIOC_IASSRT	R										IA[15:0]				IA		
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOC_IEN	R										IEN[15:0]				IEN		
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOC_IEPOL	R										IEPOL[15:0]				IEPOL		
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOC_IPEND	R										IPR[15:0]				IPR		
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOC_IEDGE	R										IES[15:0]				IES		
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOC_PPOUTM	R										OEN[15:0]				OEN		
		W																
		RS	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$A	GPIOC_RDATA	R										RAW DATA[15:0]				RAW DATA		
		W																
		RS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOC_DRIVE	R										DRIVE[15:0]				DRIVE		
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-3 GPIOC Register Map Summary

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOD_PUPEN	R													PU[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$1	GPIOD_DATA	R													D[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOD_DDIR	R													DD[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOD_PEREN	R													PE[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$4	GPIOD_IASSRT	R													IA[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOD_IEN	R													IEN[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOD_IEPOL	R													IEPOL[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOD_IPEND	R													IPR[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOD_IEDGE	R													IES[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOD_PPOUTM	R													OEN[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$A	GPIOD_RDATA	R													RAW DATA[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
$B	GPIOD_DRIVE	R													DRIVE[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-4 GPIOD Register Map Summary

Part 9 Joint Test Action Group (JTAG)

9.1 56F8023 Information

Please contact your Freescale sales representative or authorized distributor for device/package-specific BSDL information.

The $\overline{\text{TRST}}$ pin is not available in this package. The pin is tied to V_{DD} in the package.

The JTAG state machine is reset during POR and can also be reset via a soft reset by holding TMS high for five rising edges of TCK, as described in the **56F802X and 56F803X Peripheral Reference Manual**.

Part 10 Specifications

10.1 General Characteristics

The 56F8023 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels, combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40ºC to 125ºC ambient temperature over the following supply ranges:
$V_{SS} = V_{SSA} = 0V$, $V_{DD} = V_{DDA} = 3.0–3.6V$, $CL \leq 50pF$, $f_{OP} = 32MHz$

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 10-1 Absolute Maximum Ratings

(V_{SS} = 0V, V_{SSA} = 0V)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		- 0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		- 0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		- 0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Groups 1, 2	- 0.3	6.0	V
Oscillator Voltage Range	V_{OSC}	Pin Group 4	- 0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	- 0.3	4.0	V
Input clamp current, per pin (V_{IN} < 0)[1]	V_{IC}		—	-20.0	mA
Output clamp current, per pin (V_O < 0)[1]	V_{OC}		—	-20.0	mA
Output Voltage Range (Normal Push-Pull mode)	V_{OUT}	Pin Group 1	- 0.3	4.0	V
Output Voltage Range (Open Drain mode)	V_{OUTOD}	Pin Group 2	- 0.3	6.0	V
Ambient Temperature Industrial	T_A		- 40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		- 55	150	°C

1. Continuous clamp current per pin is -2.0 mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4: XTAL, EXTAL

10.1.1 ElectroStatic Discharge (ESD) Model

Table 10-2 56F8023 ESD Protection

Characteristic	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V

Table 10-2 56F8023 ESD Protection

Characteristic	Min	Typ	Max	Unit
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	750	—	—	V

Table 10-3 LQFP Package Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value (LQFP)	Unit	Notes
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	41	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	34	°C/W	1, 2
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	34	°C/W	2
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	29	°C/W	1, 2
Junction to board		$R_{\theta JB}$	24	°C/W	4
Junction to case		$R_{\theta JC}$	8	°C/W	3
Junction to package top	Natural Convection	Ψ_{JT}	2	°C/W	5

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$), was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p, where “s” is the number of signal layers and “p” is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Junction to board thermal resistance, Theta-JB ($R_{\theta JB}$), is a metric of the thermal resistance from the junction to the printed circuit board determined per JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal Characterization Parameter, Psi-JT (Y_{JT}), is the “resistance” from junction to reference point thermocouple on top center of case as defined in JESD51-2. Y_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.
6. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
7. See **Section 12.1** for more details on thermal design considerations.

Table 10-4 Recommended Operating Conditions
($V_{REFL\ x}$= 0V, V_{SSA} = 0V, V_{SS} = 0V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High	V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 1 0		 32 32	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3		0.8	V
Oscillator Input Voltage High XTAL not driven by an external clock XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	 V_{DDA} - 0.8 2.0		 V_{DDA} + 0.3 V_{DDA} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature (Extended Industrial)	T_A		-40		105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15		—	years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

1. Total chip source or sink current cannot exceed 75mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4 XTAL, EXTAL

10.2 DC Electrical Characteristics

Table 10-5 DC Electrical Characteristics
At Recommended Operating Conditions

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High (a) pull-up enabled or disabled	I_{IH}	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{IN} = 2.4V to 5.5V
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low[1] pull-up enabled pull-up disabled	I_{IL}	Pin Groups 1, 2	 -15 —	 -30 0	 -60 +/- 2.5	µA	V_{IN} = 0V
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	Internal	Typically V_{SSA} + 40mV	—	Typically V_{SSA} – 40mV	V	—
Output Current [1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 2.5	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	—	0.35	—	V	—
Input Capacitance	C_{IN}		—	10	—	pF	—
Output Capacitance	C_{OUT}		—	10	—	pF	—

1. See **Figure 10-1**

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4: XTAL, EXTAL

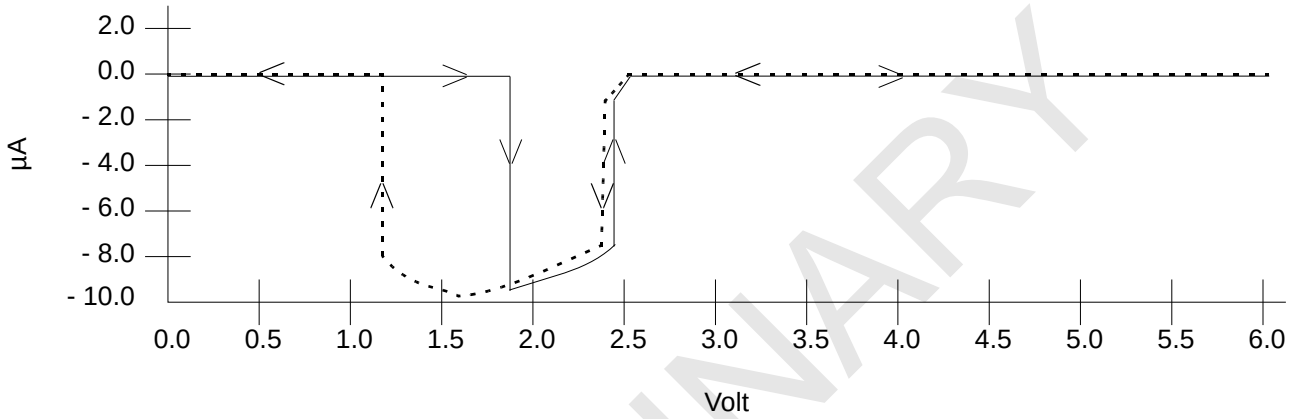


Figure 10-1 I_{IN}/I_{OZ} vs. V_{IN} (Typical; Pull-Up Disabled)

Table 10-6 Current Consumption per Power Supply Pin

Mode	Conditions	Typical @ 3.3V, 25°C		Maximum@ 3.6V, 25°C	
		I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN	32MHz Device Clock Relaxation Oscillator on PLL powered on Continuous MAC instructions with fetches from Program Flash All peripheral modules enabled. TMR and PWM using 1X Clock ADC/DAC powered on and clocked Comparator powered on	48mA	18.8mA	—	—
WAIT	32MHz Device Clock Relaxation Oscillator on PLL powered on Processor Core in WAIT state All Peripheral modules enabled. TMR and PWM using 1X Clock ADC/DAC/Comparator powered off	29mA	0µA	—	—
STOP	4MHz Device Clock Relaxation Oscillator on PLL powered off Processor Core in STOP state All peripheral module and core clocks are off ADC/DAC/Comparator powered off	5.4mA	0µA	—	—

Table 10-6 Current Consumption per Power Supply Pin (Continued)

Mode	Conditions	Typical @ 3.3V, 25°C		Maximum@ 3.6V, 25°C	
		I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
STANDBY > STOP	100kHz Device Clock Relaxation Oscillator in Standby mode PLL powered off Processor Core in STOP state All peripheral module and core clocks are off ADC/DAC/Comparator powered off Voltage regulator in Standby mode	540µA	0µA	650µA	1µA
POWERDOWN	Device Clock is off Relaxation Oscillator powered off PLL powered off Processor Core in STOP state All peripheral module and core clocks are off ADC /DAC/Comparator powered off Voltage Regulator in Standby mode	440µA	0µA	550µA	1µA

1. No Output Switching
   All ports configured as inputs
   All inputs Low
   No DC Loads

Table 10-7 Power-On Reset Low-Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3V supply[1]	$V_{EI3.3}$	2.58	2.7	—	V
Low-Voltage Interrupt for 2.5V supply[2]	$V_{E12.5}$	—	2.15	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset[3]	POR	—	1.8	1.9	V

1. When V_{DD} drops below $V_{EI3.3}$, an interrupt is generated.
2. When V_{DD} drops below $V_{EI32.5}$, an interrupt is generated.
3. Power-On Reset occurs whenever the internally regulated 2.5V digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 2.15V or the 3.3V 1/O voltage is below 2.7V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

10.2.1 Voltage Regulator Specifications

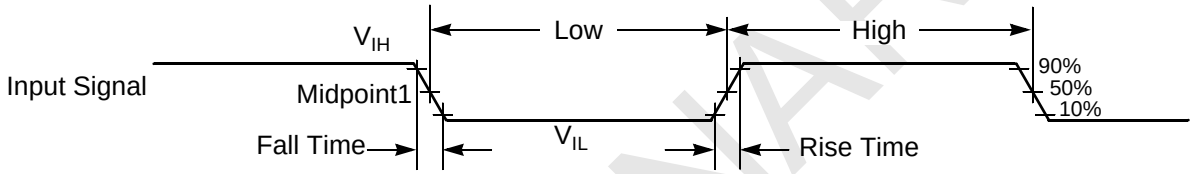
The 56F8023 has two on-chip regulators. One supplies the PLL and relaxation oscillator. It has no external pins and therefore has no external characteristics which must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5V to the 56F8023's core logic. This regulator requires an external 4.4µF, or greater, capacitor for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in **Table 10-8**.

Table 10-8. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Short Circuit Current	I_{SS}	—	450	650	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	minutes

10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-2**.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 10-2 Input Signal Measurement References

Figure 10-3 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

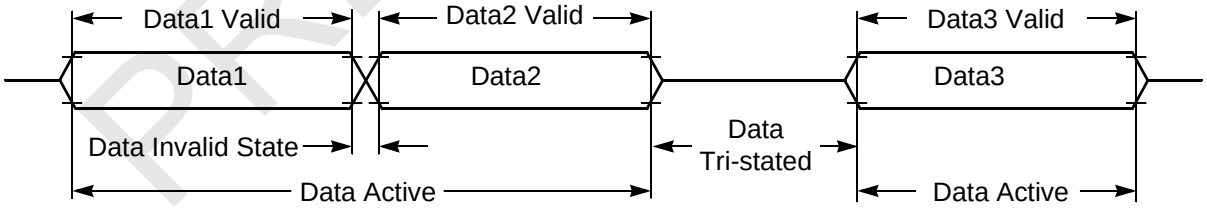


Figure 10-3 Signal States

10.4 Flash Memory Characteristics

Table 10-9 Flash Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Program time[1]	Tprog	20	—	40	µs
Erase time [2]	Terase	20	—	—	ms
Mass erase time	Tme	100	—	—	ms

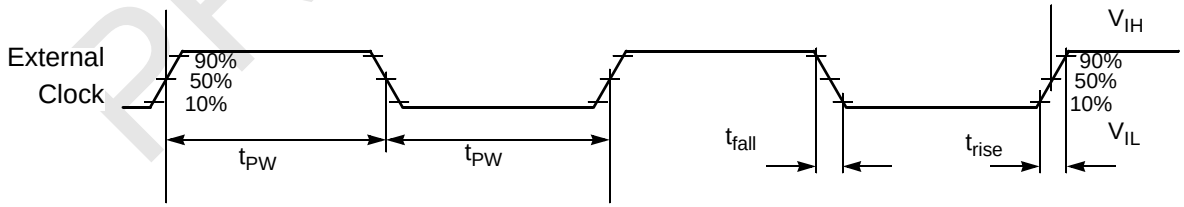
1. There is additional overhead which is part of the programming sequence. See the **56F802X and 56F803X Peripheral Reference Manual** for details.
2. Specifies page erase time. There are 512 bytes per page in the Program Flash memory.

10.5 External Clock Operation Timing

Table 10-10 External Clock Operation Timing Requirements[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[2]	f_{osc}	4	8	8	MHz
Clock Pulse Width[3]	t_{PW}	6.25	—	—	ns
External Clock Input Rise Time[4]	t_{rise}	—	—	3	ns
External Clock Input Fall Time[5]	t_{fall}	—	—	3	ns

1. Parameters listed are guaranteed by design.
2. See **Figure 10-4** for details on using the recommended connection of an external clock driver.
3. The chip may not function if the high or low pulse width is smaller than 6.25ns.
4. External clock input rise time is measured from 10% to 90%.
5. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 10-4 External Clock Timing

10.6 Phase Locked Loop Timing

Table 10-11 PLL Timing

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	4	8	—	MHz
Internal reference relaxation oscillator frequency for the PLL	f_{rosc}	—	8	—	MHz
PLL output frequency[2] (24 x reference frequency)	f_{op}	96	192	—	MHz
PLL lock time[3]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8MHz external crystal as the PLL source[4]	J_A	—	—	0.37	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input.
2. The core system clock will operate at 1/6 of the PLL output frequency.
3. This is the time required after the PLL is enabled to ensure reliable operation.
4. This is measured on the CLKO signal (programmed as System clock) over 264 System clocks at 32MHz System clock frequency and using an 8MHz oscillator frequency.

10.7 Relaxation Oscillator Timing

Table 10-12 Relaxation Oscillator Timing

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
Relaxation Oscillator output frequency[1] Normal Mode Standby Mode	f_{op}	—	 8.05 200	—	 MHz kHz
Relaxation Oscillator stabilization time[2]	t_{roscs}	—	1	3	ms
Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks[3]	$t_{jitterrosc}$	—	400	—	ps
Minimum tuning step size		—	.08	—	%
Maximum tuning step size		—	40	—	%
Variation over temperature -40°C to 150ºC[4]		—	+1.0 to -1.5	+3.0 to -3.0	%
Variation over temperature 0°C to 105ºC[4]		—	0 to +1	+2.0 to -2.0	%

1. Output frequency after factory trim.
2. This is the time required from Standby to Normal mode transition.
3. J_A is required to meet QSCI requirements.
4. See **Figure 10-5**

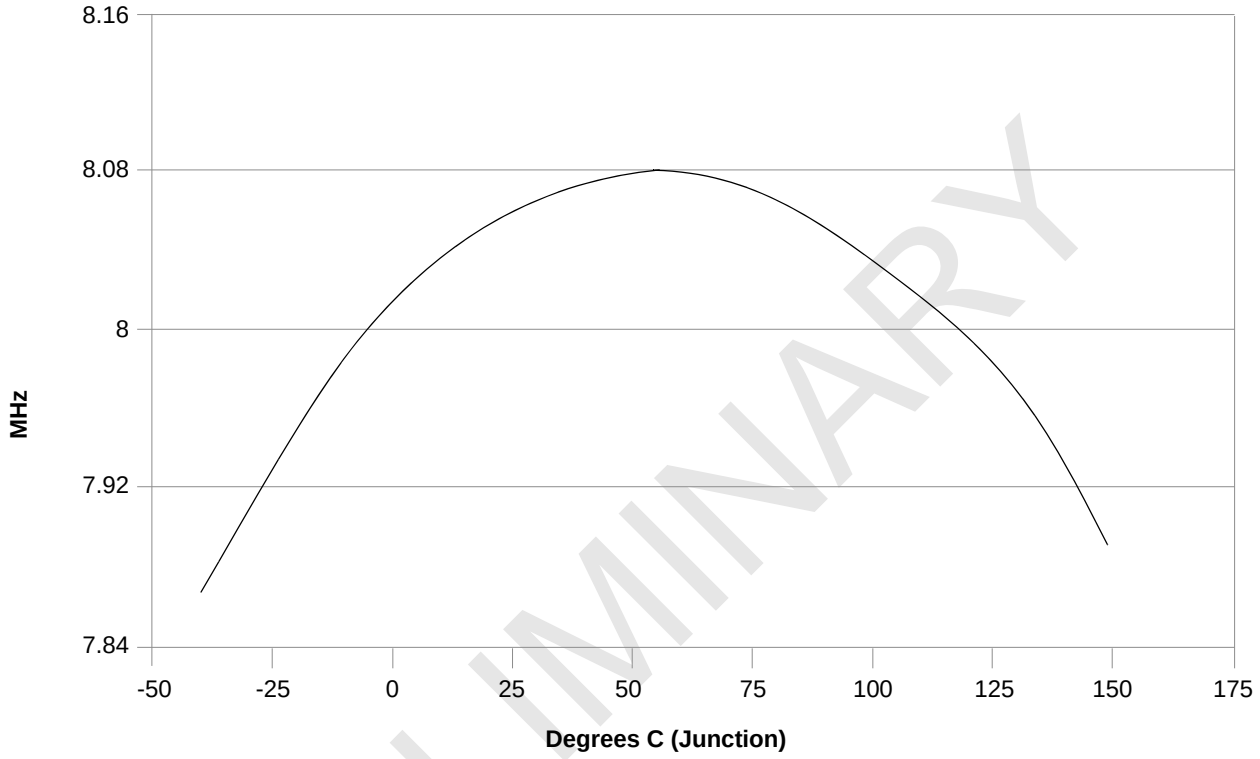


Figure 10-5 Relaxation Oscillator Temperature Variation (Typical) After Trim

10.8 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Note: All address and data buses described here are internal.

Table 10-13 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	4T	—	ns	—
Minimum GPIO pin Assertion for Interrupt	t_{IW}	2T	—	ns	10-6
$\overline{\text{RESET}}$ deassertion to First Address Fetch[3]	t_{RDA}	$96T_{OSC}$ + 64T	$97T_{OSC}$ + 65T	ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	—	6T	ns	—

1. In the formulas, T = system clock cycle and T_{osc} = oscillator clock cycle. For an operating frequency of 32MHz, T = 31.25ns. At 8MHz (used during Reset and Stop modes), T = 125ns.
2. Parameters listed are guaranteed by design.
3. During Power-On Reset, it is possible to use the 56F8023 internal reset stretching circuitry to extend this period to 2^21T.

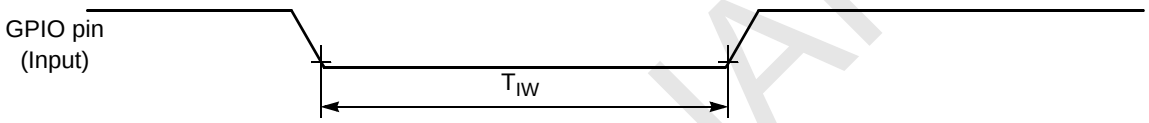


Figure 10-6 GPIO Interrupt Timing (Negative Edge-Sensitive)

10.9 Serial Peripheral Interface (SPI) Timing

Table 10-14 SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	10-10
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	10-10
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	10-10
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	10-10
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	10-10
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	10-7, 10-8, 10-9, 10-10
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	10-7, 10-8, 10-9, 10-10
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	10-7, 10-8, 10-9, 10-10

1. Parameters listed are guaranteed by design.

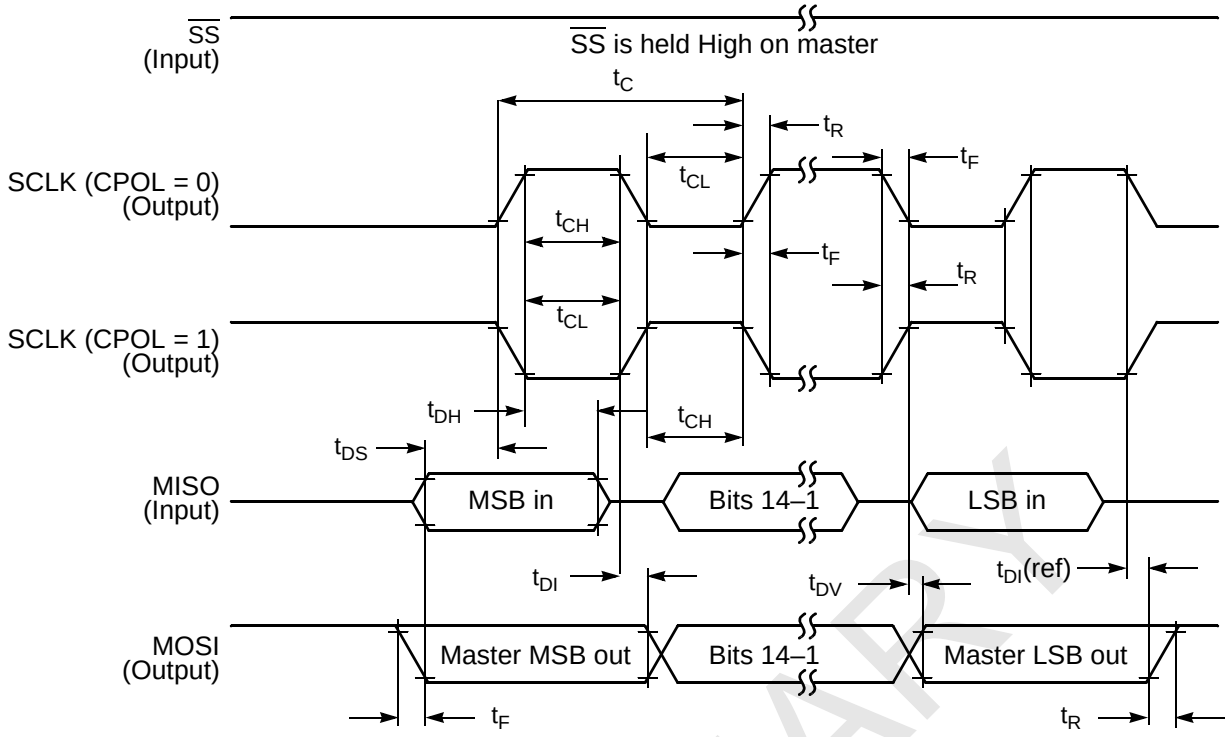


Figure 10-7 SPI Master Timing (CPHA = 0)

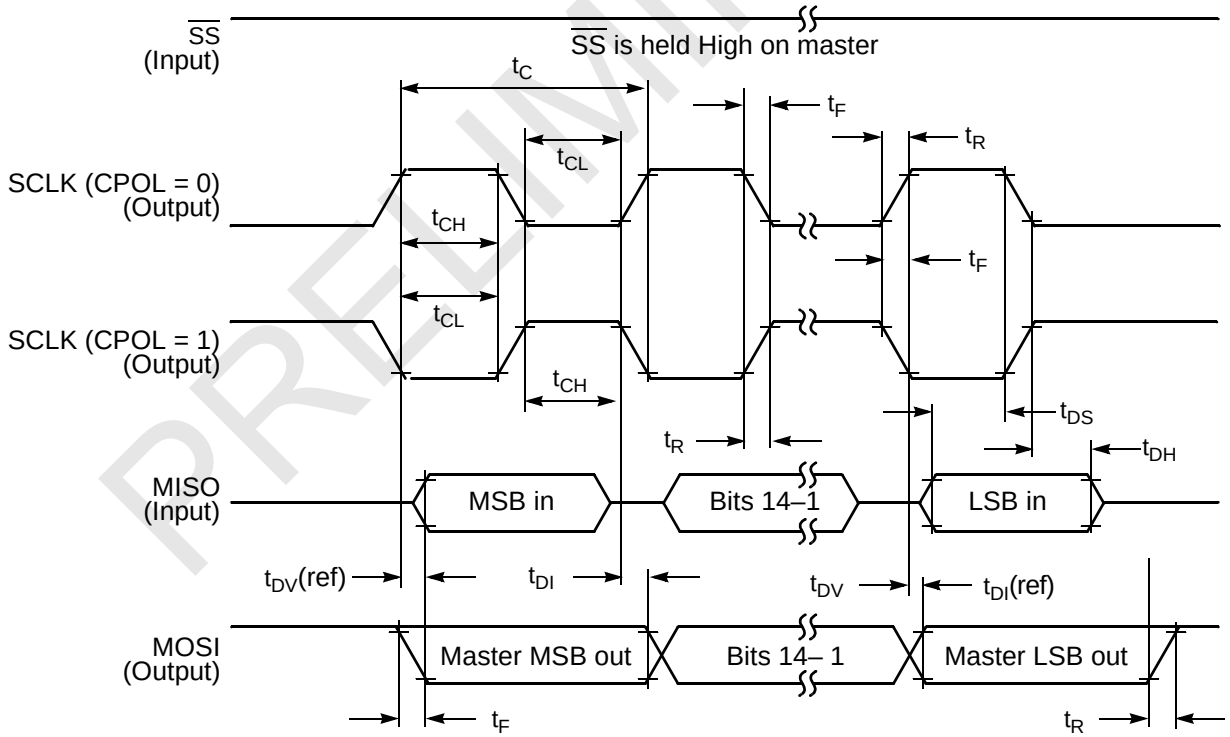


Figure 10-8 SPI Master Timing (CPHA = 1)

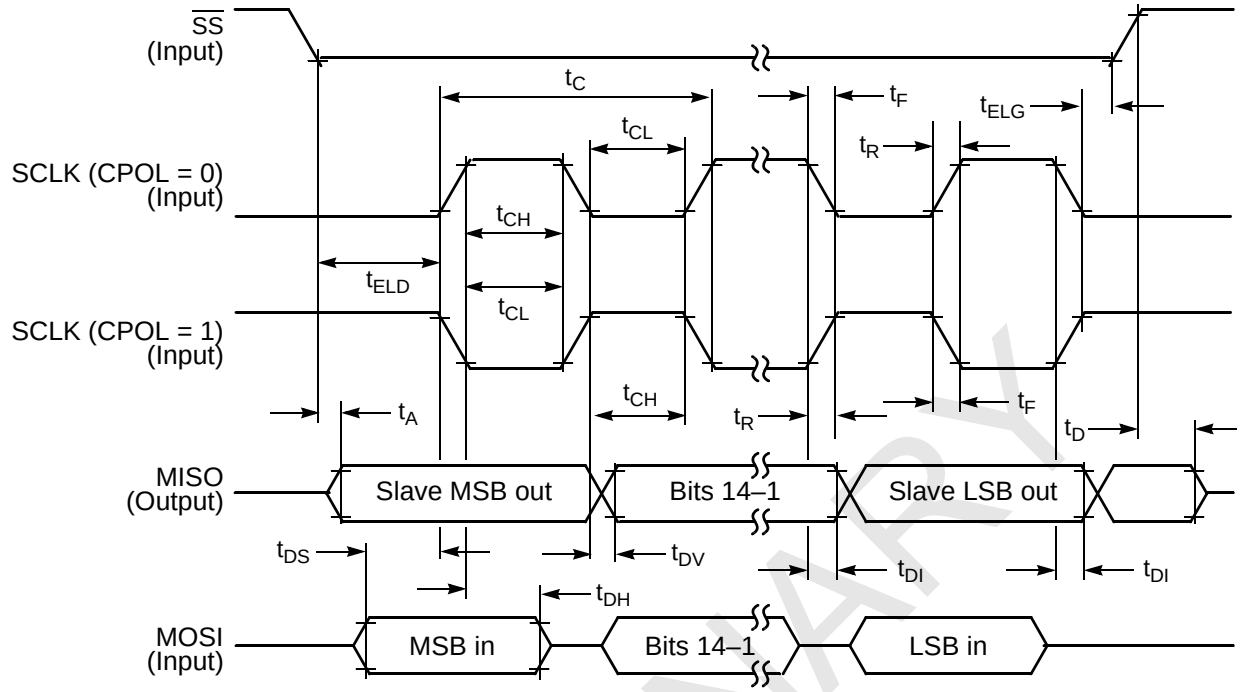


Figure 10-9 SPI Slave Timing (CPHA = 0)

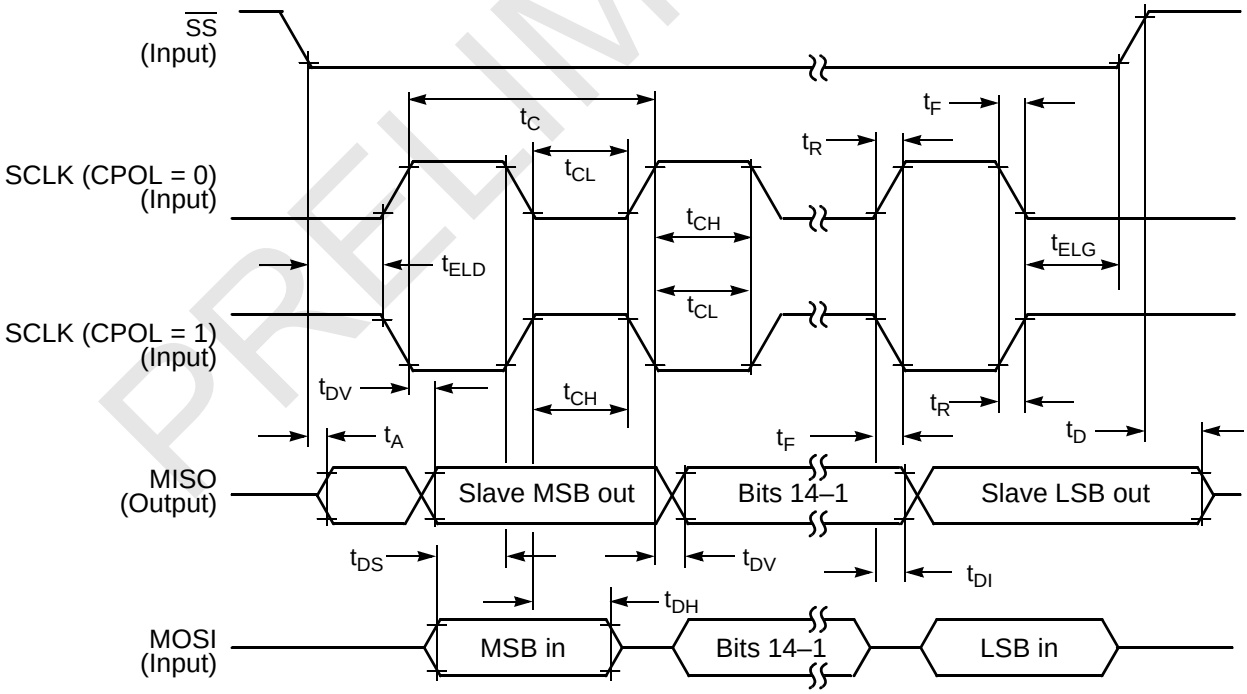


Figure 10-10 SPI Slave Timing (CPHA = 1)

10.10 Quad Timer Timing

Table 10-15 Timer Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	10-11
Timer input high / low period	P_{INHL}	1T + 3	—	ns	10-11
Timer output period	P_{OUT}	125	—	ns	10-11
Timer output high / low period	P_{OUTHL}	50	—	ns	10-11

1. In the formulas listed, T = the clock cycle. For 32MHz operation, T = 31.25ns.
2. Parameters listed are guaranteed by design.

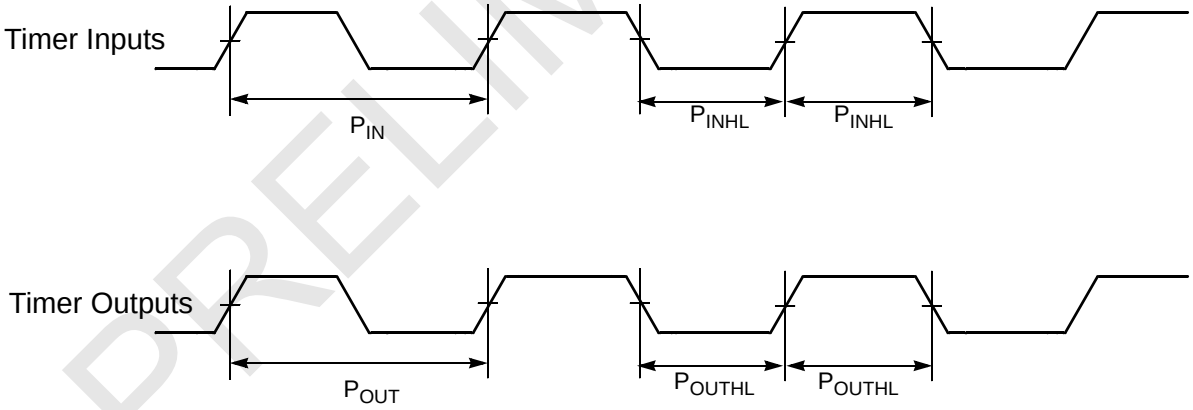


Figure 10-11 Timer Timing

10.11 Serial Communication Interface (SCI) Timing

Table 10-16 SCI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate[2]	BR	—	(f_{MAX}/16)	Mbps	—
RXD[3] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns	10-12
TXD[4] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns	10-13
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. Parameters listed are guaranteed by design.
2. f_{MAX} is the frequency of operation of the system clock in MHz, which is 32MHz for the 56F8023 device.
3. The RXD pin in QSCI0 is named RXD0 and the RXD pin in QSCI1 is named RXD1.
4. The TXD pin in QSCI0 is named TXD0 and the TXD pin in QSCI1 is named TXD1.

Figure 10-12 RXD Pulse Width

Figure 10-13 TXD Pulse Width

10.12 Inter-Integrated Circuit Interface (I^2C) Timing

Table 10-17 I^2C Timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	0[1]	0.9[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250[3]	—	100[3, 4]	—	ns
Rise time of both SDA and SCL signals	t_r	—	1000	20 +0.1C_b[5]	300	ns
Fall time of both SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
4. A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT}$ > = 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
5. C_b = total capacitance of the one bus line in pF.

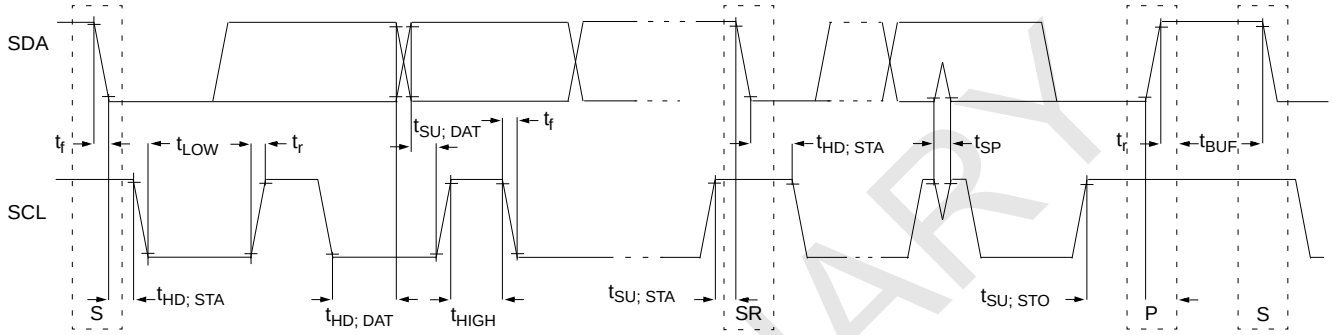


Figure 10-14 Timing Definition for Fast and Standard Mode Devices on the I^2C Bus

10.13 JTAG Timing

Table 10-18 JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation[1]	f_{OP}	DC	SYS_CLK/8	MHz	10-15
TCK clock pulse width	t_{PW}	50	—	ns	10-15
TMS, TDI data set-up time	t_{DS}	5	—	ns	10-16
TMS, TDI data hold time	t_{DH}	5	—	ns	10-16
TCK low to TDO data valid	t_{DV}	—	30	ns	10-16
TCK low to TDO tri-state	t_{TS}	—	30	ns	10-16

1. TCK frequency of operation must be less than 1/8 the processor rate.

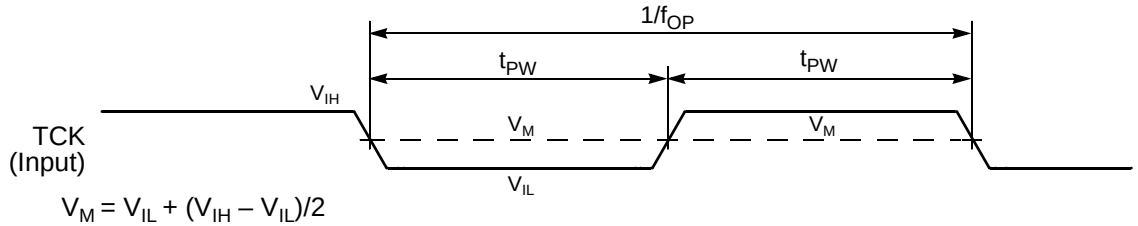


Figure 10-15 Test Clock Input Timing Diagram

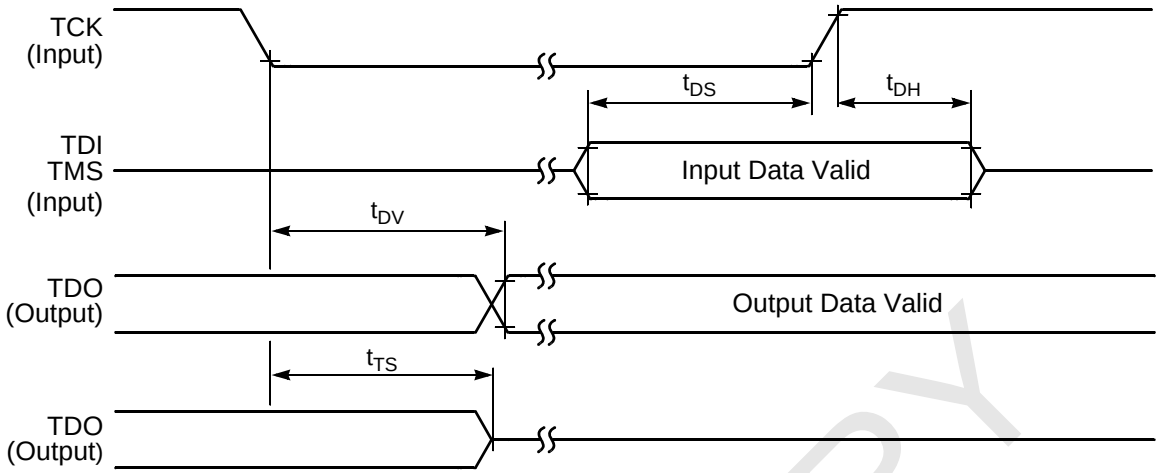


Figure 10-16 Test Access Port Timing Diagram

10.14 Analog-to-Digital Converter (ADC) Parameters

Table 10-19 ADC Parameters[1]

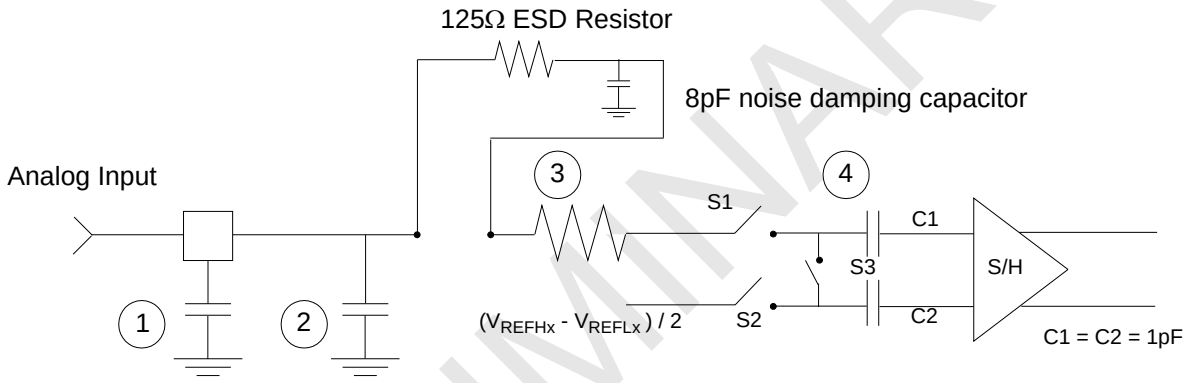
Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	5.33	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC power-up time[2]	t_{ADPU}	—	6	13	t_{AIC} cycles[3]
Recovery from auto standby	t_{REC}	—	0	1	t_{AIC} cycles[3]
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy					
Integral non-linearity[4] (Full input signal range)	INL	—	+/- 3	+/- 5	LSB[5]
Differential non-linearity	DNL	—	+/- .6	+/- 1	LSB[5]
Monotonicity			GUARANTEED		
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 4	+/- 9	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 6	+/- 12	mV
Gain Error (transfer gain)	E_{GAIN}	—	.998 to 1.002	1.01 to .99	—
ADC Inputs[6] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0	—	µA
Input injection current[7], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See **Figure 10-17**	—	pF
Input impedance	X_{IN}	—	See **Figure 10-17**	—	Ohms
AC Specifications					
Signal-to-noise ratio	SNR	60	65		dB
Total Harmonic Distortion	THD	60	64		dB
Spurious Free Dynamic Range	SFDR	61	66		dB
Signal-to-noise plus distortion	SINAD	58	62		dB
Effective Number Of Bits	ENOB	—	10.0		Bits

1. All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2. Includes power-up of ADC and V_{REF}
3. ADC clock cycles
4. INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
5. LSB = Least Significant Bit = 0.806mV
6. Pin groups are detailed following **Table 10-1**.
7. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC.

10.15 Equivalent Circuit for ADC Inputs

Figure 10-17 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to (V_{REFHx}- V_{REFLx}) / 2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about (V_{REFHx}-V_{REFLx}) / 2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF}, and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. Equivalent resistance for the channel select mux; 100 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF

Figure 10-17 Equivalent Circuit for A/D Loading

10.16 Comparator (CMP) Parameters

Table 10-20 CMP Parameters

Characteristic	Conditions/Comments	Symbol	Min	Typ	Max	Unit
Input Offset Voltage[1]	Within range of V_{DDA} - .1V to V_{SSA} + .1V	V_{OFFSET}	—	± 10	± 35	mV
Input Propagation Delay		t_{PD}	—	35	45	ns
Power-up time		t_{CPU}	—	TBD	TBD	

1. No guaranteed specification within 0.1V of V_{DDA} or V_{SSA}

10.17 Digital-to-Analog Converter (DAC) Parameters

Table 10-21 DAC Parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12		12	bits
Conversion time			TBD	—	2	µS
Conversion rate			TBD	—	500.000	conv/sec
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µS
Accuracy						
Integral non-linearity[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	INL	—	+/- 3	+/- 8.0	LSB[2]
Differential non-linearity[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- .8	< - 1	LSB[2]
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity			guaranteed		—
Offset error[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+/- 25	+/- 40	mV
Gain error[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- .5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40mV of either V_{REFLX} or V_{REFHX}	V_{OUT}	V_{REFLX} +.04V	—	V_{REFHX} - .04V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	TBD	—	dB
Spurious free dynamic range		SFDR	—	TBD	—	dB
Effective number of bits		ENOB	9	—	—	bits

1. No guaranteed specification within 5% of V_{DDA} or V_{SSA}
2. LSB = 0.806mV

10.18 Power Consumption

See **Section 10.1** for a list of IDD requirements for the 56F8023. This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]
+B: internal [state-dependent component]
+C: internal [dynamic component]
+D: external [dynamic component]
+E: external [static component]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

C, the internal [dynamic component], is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic component], reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 10-22 I/O Loading Coefficients at 10MHz

	Intercept	Slope
8mA drive	1.3	0.11mW / pF
4mA drive	1.15mW	0.11mW / pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. **Table 10-22** provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases:

$$TotalPower = \Sigma((\text{Intercept} + \text{Slope}*\text{Cload})*\text{frequency}/10\text{MHz})$$

where:

- Summation is performed over all output pins with capacitive loads
- TotalPower is expressed in mW
- Cload is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

Part 11 Packaging

11.1 56F8023 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8023. This device comes in a 32-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline, **Figure 11-2** shows the mechanical parameters and **Table 11-1** lists the pin-out.

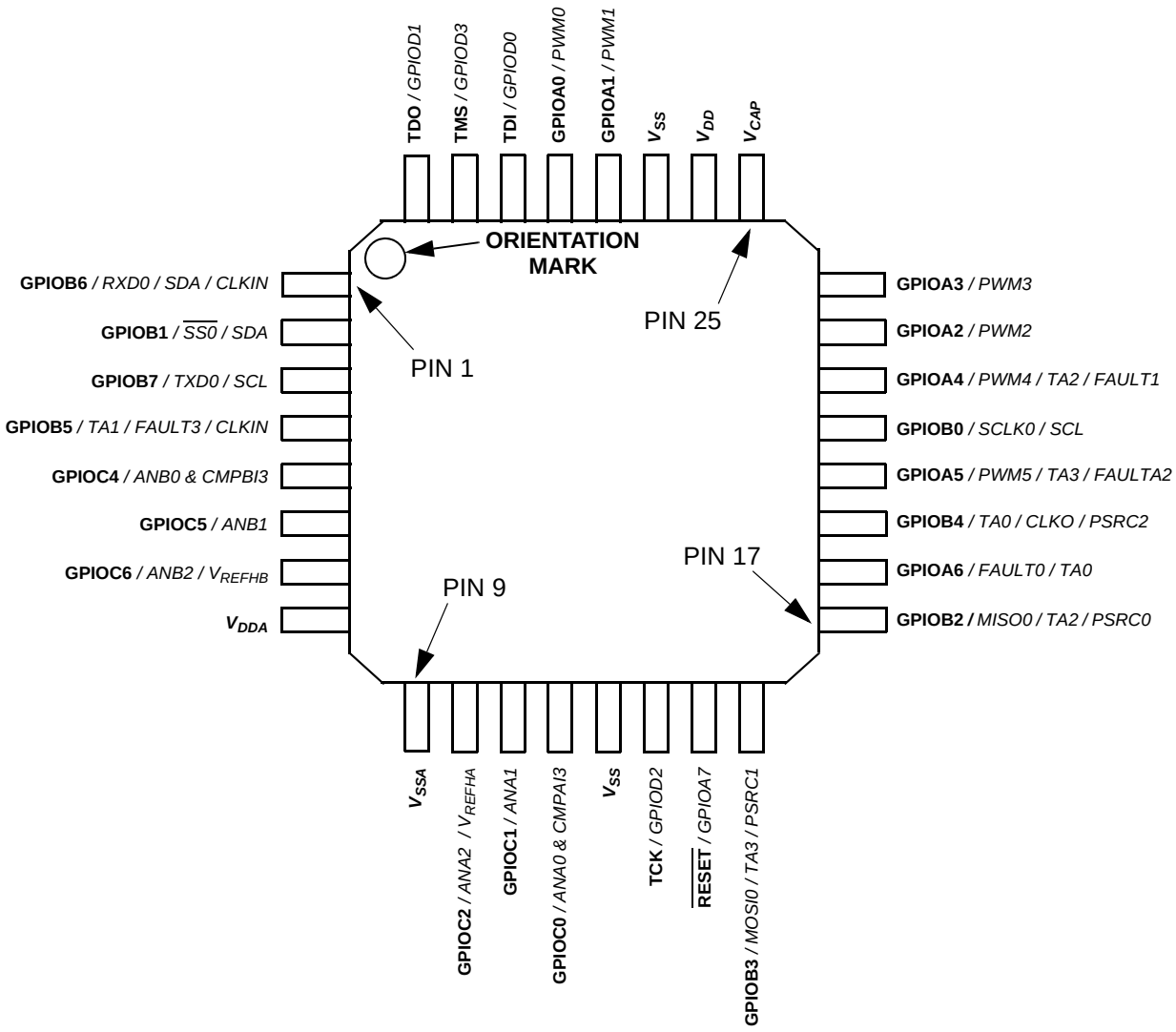
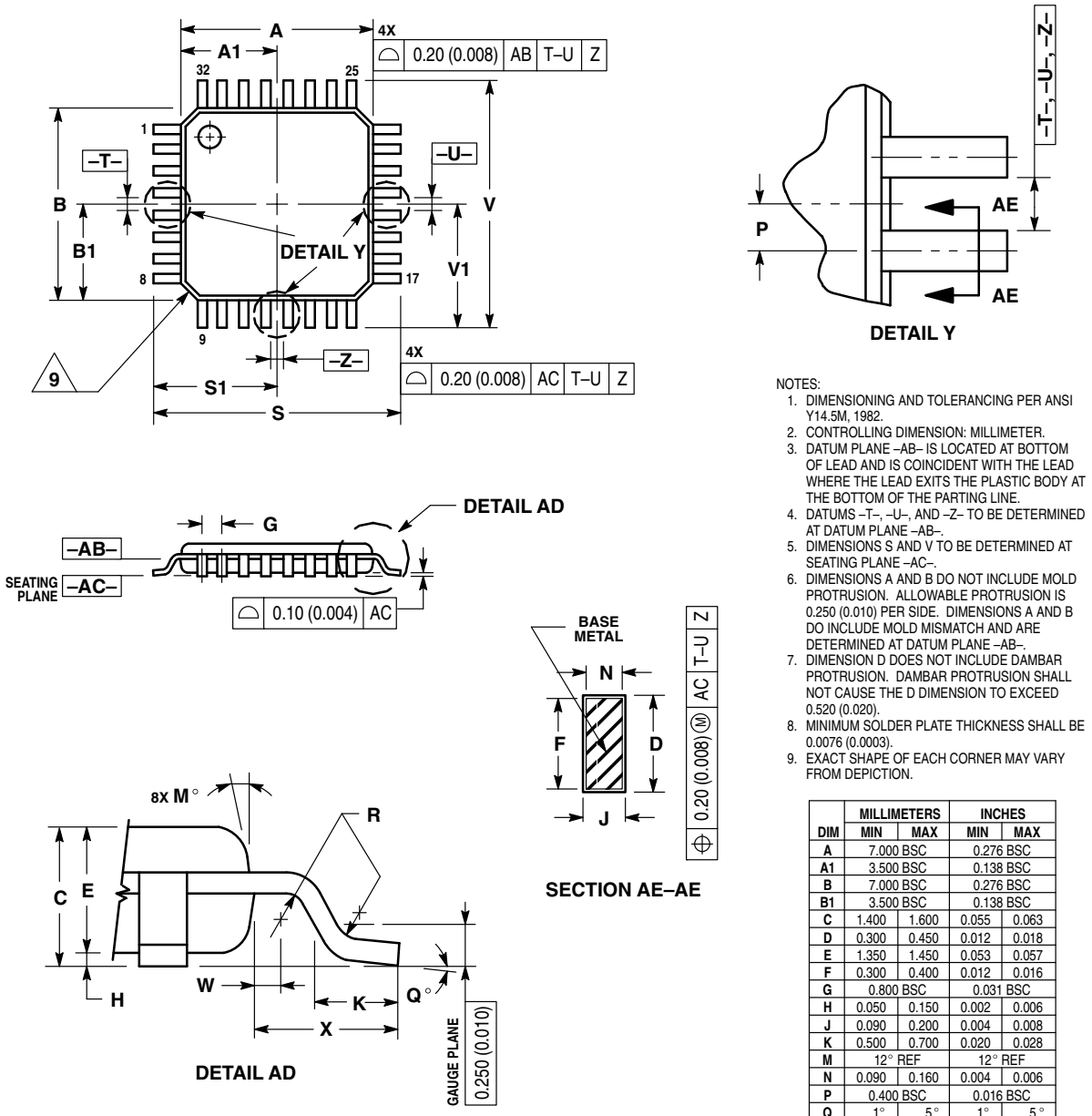


Figure 11-1 Top View, 56F8023 32-Pin LQFP Package

Table 11-1 56F8023 32-Pin LQFP Package Identification by Pin Number[1]

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	**GPIOB6** *RXD0 / SDA / CLKIN*	9	**V_{SSA}**	17	**GPIOB2** *MISO0 / TA2 / PSRC0*	25	**V_{CAP}**
2	**GPIOB1** *$\overline{SS0}$ / SDA*	10	**GPIOC2** *ANA2 / V_{REFHA}*	18	**GPIOA6** *FAULT0 / TA0*	26	**V_{DD}**
3	**GPIOB7** *TXD0 / SCL*	11	**GPIOC1** *ANA1*	19	**GPIOB4** *TA0 / CLKO / PSRC2*	27	**V_{SS}**
4	**GPIOB5** *TA1 / FAULT3 / CLKIN*	12	**GPIOC0** *ANA0 & CMPAI3*	20	**GPIOA5** *PWM5 / TA3 / FAULT2*	28	**GPIOA1** *PWM1*
5	**GPIOC4** *ANB0 & CMPBI3*	13	**V_{SS}**	21	**GPIOB0** *SCLK0 / SCL*	29	**GPIOA0** *PWM0*
6	**GPIOC5** *ANB1*	14	**TCI** *GPIOD2*	22	**GPIOA4** *PWM4 / TA2 / FAULT1*	30	**TDI** *GPIOD0*
7	**GPIOC6** *ANB2 / V_{REFHB}*	15	**$\overline{RESET}$** *GPIOA7*	23	**GPIOA2** *PWM2*	31	**TMS** *GPIOD3*
8	**V_{DDA}**	16	**GPIOB3** *MOSI0 / TA3 / PSRC1*	24	**GPIOA3** *PWM3*	32	**TDO** *GPIOD1*

1. Alternate signals are in italic



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Figure 11-2 56F8023 32-Pin LQFP Mechanical Information

Please see **www.freescale.com** for the most current case outline.

Part 12 Design Considerations

12.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$
where:

T_A = Ambient temperature for the package (^oC)
$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)
P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$
where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = Package junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$
where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter ($^oC/W$)
P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8023:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the 56F8023 and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible
- Bypass the V_{DD} and V_{SS} with approximately 100µF, plus the number of 0.1µF ceramic capacitors
- PCB trace lengths should be minimal for high-frequency signals
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.

- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as close as possible to power supply outputs. If both analog circuit and digital circuit are powered by the same power supply, it is advisable to connect a small inductor or ferrite bead in serial with both V_{DDA} and V_{SSA} traces.
- It is highly desirable to physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. It is also desirable to place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the Flash memory is programmed through the JTAG/EOnCE port, QSPI, QSCI, or I^2C, the designer should provide an interface to this port if in-circuit Flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The Resistor value should be in the range of 4.7k—10k; the Capacitor value should be in the range of 0.22µf - 4.7µf.
- Add a 3.3k external pull-up on the TMS pin of the JTAG port to keep EOnce in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input state with internal pull-up enable. The typical value of internal pull-up is around 110K. These internal pull-ups can be disabled by software.
- To eliminate PCB trace impedance effect, each ADC input should have a 33pf-10 ohm RC filter.
- Device GPIOs have only a down (substrate) diode on the GPIO circuit. Devices do not have a positive clamp diode because GPIOs use a floating gate structure to tolerate 5V input. The absolute maximum clamp current is -20mA at V_{in} less than 0V. The continuous clamp current is -2mA at V_{in} less than 0V. If positive voltage spikes are a concern, a positive clamp is recommended.

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order devices.

Table 13-1 56F8023 Ordering Information

Device	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8023	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	32	32	-40° to + 105° C	MC56F8023VLC*

* This package is RoHS compliant.

Part 14 Appendix

Register acronyms are revised from previous device data sheets to provide a cleaner register description. A cross reference to legacy and revised acronyms are provided in the following table.

Note: This table comprises all peripherals used in the 56F803x and 56F802x family; some of the peripherals described here may not be present on this device.

Table 14-1 Legacy and Revised Acronyms

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Analog-to-Digital Converter (ADC) Module							
Control 1 Register	CTRL1	ADCR1	ADC_CTRL1	ADC_ADCR1	ADC_ADCR1	0xF080	
Control 2 Register	CTRL2	ADCR2	ADC_CTRL2	ADC_ADCR2	ADC_ADCR2	0xF081	
Zero Crossing Control Register	ZXCTRL	ADZCC	ADC_ZXCTRL	ADC_ADZCC	ADC_ADZCC	0xF082	
Channel List 1 Register	CLIST1	ADLST1	ADC_CLIST1	ADC_ADLST1	ADC_ADLST1	0xF083	
Channel List 2 Register	CLIST2	ADLST2	ADC_CLIST2	ADC_ADLST2	ADC_ADLST2	0xF084	
Channel List 3 Register	CLIST3		ADC_CLIST3	ADC_ADCLST3	ADC_ADCLST3	0xF085	
Channel List 4 Register	CLIST4		ADC_CLIST4	ADC_ADCLST4	ADC_ADCLST4	0xF086	
Sample Disable Register	SDIS	ADSDIS	ADC_SDIS	ADC_ADSDIS	ADC_ADSDIS	0xF087	
Status Register	STAT	ADSTAT	ADC_STAT	ADC_ADSTAT	ADC_ADSTAT	0xF088	
Conversion Ready Register	RDY		ADC_CNRDY	ADC_ADCNRDY	ADC_ADCNRDY	0xF089	
Limit Status Register	LIMSTAT	ADLSTAT	ADC_LIMSTAT	ADC_ADLSTAT	ADC_ADLSTAT	0xF08A	
Zero Crossing Status Register	ZXSTAT	ADZCSTAT	ADC_ZXSTAT	ADC_ADZCSTAT	ADC_ADZCSTAT	0xF08B	
Result 0-7 Registers	RSLT0-7	ADRSLT0-7	ADC_RSLT0-7	ADC_ADRSLT0-7	ADC_ADRSLT0-7	0xF08C	0XF093
Result 8-15 Registers	RSLT8-15		ADC_RSLT8-15	ADC_ADRSLT8-15	ADC_ADRSLT8-15	0xF094	0XF09B
Low Limit 0-7 Registers	LOLIM0-7	ADLLMT0-7	ADC_LOLIM0-7	ADC_ADLLMT0-7	ADC_ADLLMT0-7	0XF09C	0XF0A3
High Limit 0-7 Registers	HILIM0-7	ADHLMT0-7	ADC_HILIM0-7	ADC_ADHLMT0-7	ADC_ADHLMT0-7	0XF0A4	0XF0AB
Offset 0-7 Registers	OFFST0-7	ADOFS0-7	ADC_OFFST0-7	ADC_ADOFS0-7	ADC_ADOFS0-7	0XF0AC	0XF0B3
Power Control Register	PWR	ADPOWER	ADC_PWR	ADC_ADPOWER	ADC_ADPOWER	0XF0B4	
Calibration Register	CAL		ADC_CAL	ADC_ADCAL	ADC_ADCAL	0XF0B5	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Computer Operating Properly (COP) Module							
Control Register	CTRL	COPCTL	COP_CTRL	COPCTL	COPCTL	0XF120	
Timeout Register	TOUT	COPTO	COP_TOUT	COPTO	COPTO	0XF121	
Counter Register	CNTR	COPCTR	COP_CNTR	COPCTR	COPCTR	0XF122	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Inter-Integrated Circuit Interface (I^2C) Module							
Control Register	CTRL	IBCR	I2C_CTRL	I2C_IBCR	I2C_IBCR	0xF280	
Target Address Register	TAR		I2C_TAR	I2CTAR	I2C_TAR	0xF282	
Slave Address Register	SAR		I2C_SAR	I2CSAR	I2C_SAR	0xF242	
Data Buffer & Command Register	DATA		I2C_DATA	I2C_DATACMD	I2C_DATACMD	0xF288	
Standard Speed Clock SCL High Count Register	SSHCNT		I2C_SS_SCL_HCNT	I2C_SS_SCLHCNT	I2C_SS_SCLHCNT	0xF28A	
Standard Speed Clock SCL Low Count Register	SSLCNT		I2C_SS_SCL_LCNT	I2C_SS_SCLLCNT	I2C_SS_SCLLCNT	0xF28C	
Fast Speed Clock SCL High Count Register	FSHCNT		I2C_FS_SCL_HCNT	I2C_FS_SCLHCNT	I2C_FS_SCLHCNT	0xF28E	
Fast Speed Clock SCL Low Count Register	FSLCNT		I2C_FS_SCL_LCNT	I2C_FS_SCLLCNT	I2C_FS_SCLLCNT	0xF290	
Interrupt Status Register	ISTAT		I2C_INTR_STAT	I2C_INTRSTAT	I2C_INTRSTAT	0xF296	
Interrupt Mask Register	IENBL		I2C_INTR_MASK	I2C_INTRMASK	I2C_INTRMASK	0xF298	
Raw Interrupt Status Register	RISTAT		I2C_RAW_INTR_STAT	I2C_RAW_INTRSTAT	I2C_RAW_INTRSTAT	0xF29A	
Receive FIFO Threshold Level Register	RXFT		I2C_RXTL		I2C_RXTL	0xF29C	
Transmit FIFO Threshold Level Register	TXFT		I2C_TXTL		I2C_TXTL	0xF29E	
Clear Combined & Individual Interrupts Register	CLRINT		I2C_CLRINTR		I2C_CLRINTR	0xF2A0	
Clear Receive Under Interrupt Register	CLRRXUND		I2C_CLR_RXUNDER		I2C_CLR_RXUNDER	0xF2A2	
Clear Receive Over Interrupt Register	CLRRXOVR		I2C_CLROVER		I2C_CLROVER	0xF2A4	
Clear Transmit Over Register	CLRTXOVR		I2C_CLR_TXOVER		I2C_CLR_TXOVER	0xF2A6	
Clear Read Required Interrupt Register	CLRRDREQ		I2C_CLR_RDREQ		I2C_CLR_RDREQ	0xF2A8	
Clear Transmit Abort Interrupt Register	CLRTXABRT		I2C_CLR_TXABRT		I2C_CLR_TXABRT	0xF2AA	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Clear Receive Done Interrupt Register	CLRRXDONE		I2C_CLR_RXDONE		I2C_CLR_RXDONE	0xF2AC	
Clear Activity Interrupt Register	CLRACT		I2C_CLRACTIVITY		I2C_CLRACTIVITY	0xF2AE	
Clear Stop Detect Interrupt Register	CLRSTPDET		I2C_CLR_STOPDET		I2C_CLR_STOPDET	0xF2B0	
Clear Start Detect Interrupt Register	CLRSTDET		I2C_CLR_STAR_DET		I2C_CLR_STAR_DET	0xF2B2	
Clear General Call Interrupt Register	CLRGC		I2C_CLR_GENCALL		I2C_CLR_GENCALL	0xF2B4	
Enable Register	ENBL		I2C_ENABLE		I2C_ENABLE	0xF2B6	
Status Register	STAT		I2C_STAT		I2C_STAT	0xF2B8	
Transmit FIFO Level Register	TXFLR		I2C_TXFLR		I2C_TXFLR	0xF2BA	
Receive FIFO Level Register	RXFLR		I2C_RXFLR		I2C_RXFLR	0xF2BC	
Transmit Abort Source Register	TXABRTSRC		I2C_TX_ABRTSRC		I2C_TX_ABRTSRC	0xF2C0	
Component Parameter 1 Register	COMPARM1		I2C_COMPARM1		I2C_COMPARM1	0xF2FA	
Component Parameter 2 Register	COMPARM2		I2C_COMPARM2		I2C_COMPARM2	0xF2FB	
Component Version 1 Register	COMVER1		I2C_COMVER1		I2C_COMVER1	0xF2FC	
Component Version 2 Register	COMVER2		I2C_COMVER2		I2C_COMVER2	0xF2FD	
Component Type 1 Register	COMTYP1		I2C_COMTYP1		I2C_COMTYP1	0xF2FE	
Component Type 2 Register	COMTYP2		I2C_COMTYP2		I2C_COMTYP2	0xF2FF	
On-Clock Chip Synthesis (OCCS) Module							
Control Register	CTRL	PLLCR	OCCS_CTRL	PLLCR	PLLCR	0xF130	
Divide-By Register	DIVBY	PLLDB	OCCS_DIVBY	PLLDB	PLLDB	0xF131	
Status Register	STAT	PLLSR	OCCS_STAT	PLLSR	PLLSR	0xF132	
Oscillator Control Register	OCTRL	OSCTL	OCCS_OCTRL	OSCTL	OSCTL	0xF135	
Clock Check Register	CLKCHK		OCCS_CLCHK	PLLCLCHK	OCCS_CLCHK	0xF136	
Protection Register	PROT		OCCS_PROT	PLLPROT	OCCS_PROT	0xF137	
Clock Divider Register	CLKDIV	FMCLKD	FM_CLKDIV	FMCLKD	FMCLKD	0xF400	
Configuration Register	CNFG	FMCR	FM_CNFG	FMCR	FMCR	0xF401	
Security High Half Register	SECHI	FMSECH	FM_SECHI	FMSECH	FMSECH	0xF403	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Security Low Half Register	SECLO	FMSECL	FM_SECLO	FMSECL	FMSECL	0xF404	
Protection Register	PROT	FMPROT	FM_PROT	FMPROT	FMPROT	0xF410	
User Status Register	USTAT	FMUSTAT	FM_USTAT	FMUSTAT	FMUSTAT	0xF413	
Command Register	CMD	FMCMD	FM_CMD	FMCMD	FMCMD	0xF414	
Data Buffer Register	DATA	FMDATA	FM_DATA	FMDATA	FMDATA	0xF418	
Info Optional Data 1 Register	OPT1	FMOPT1	FM_OPT1	FMOPT1	FMOPT1	0xF41B	
Test Array Signature Register	TSTSIG	FMTST_SIG	FM_TSTSIG	FMTST_SIG	FMTST_SIG	0xF41D	
General Purpose Input/Output (GPIO) Module							
					x = A (***n***=0) B (***n***=1) C (***n***=2) D (***n***=3)		
Pull-Up Enable Register	PUPEN	PUR	GPIO***x***_PUPEN	GPIO***x***_PUR	GPIO_***x***_PUR	0xF1***n***0	
Data Register	DATA	DR	GPIO***x***_DATA	GPIO***x***_DR	GPIO_***x***_DR	0xF1***n***1	
Data Direction Register	DDIR	DDR	GPIO***x***_DDIR	GPIO***x***_DDR	GPIO_***x***_DDR	0xF1***n***2	
Peripheral Enable Register	PEREN	PER	GPIO***x***_PEREN	GPIO***x***_PER	GPIO_***x***_PER	0xF1***n***3	
Interrupt Assert Register	IASSRT	IAR	GPIO***x***_IASSRT	GPIO***x***_IAR	GPIO_***x***_IAR	0xF1***n***4	
Interrupt Enable Register	IEN	IENR	GPIO***x***_IEN	GPIO***x***_IENR	GPIO_***x***_IENR	0xF1***n***5	
Interrupt Polarity Register	IPOL	IPOLR	GPIO***x***_IPOL	GPIO***x***_IPOLR	GPIO_***x***_IPOLR	0xF1***n***6	
Interrupt Pending Register	IPEND	IPR	GPIO***x***_IPEND	GPIO***x***_IPR	GPIO_***x***_IPR	0xF1***n***7	
Interrupt Edge-Sensitive Register	IEDGE	IESR	GPIO***x***_IEDGE	GPIO***x***_IESR	GPIO_***x***_IESR	0xF1***n***8	
Push-Pull Mode Registers	PPOUTM	PPMODE	GPIOx_PPOUTM	GPIO***x***_PPMODE	GPIO_***x***_PPMODE	0xF1***n***9	
Raw Data Input Register	RDATA	RAWDATA	GPIO***x***_RDATA	GPIOx_RAWDATA	GPIO_***x***_RAWDATA	0xF1***n***A	
Output Drive Strength Register	DRIVE	DRIVE	GPIO***x***_DRIVE	GPIO***x***_DRIVE	GPIO_***x***_DRIVE	0xF1***n***B	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Pulse Width Modulator (PWM) Module							
Control Register	CTRL	PMCTL	PWM_CTRL	PWM_PMCTL	PWM_PMCTL	0xF0C0	
Fault Control Register	FCTRL	PMFCTL	PWM_FCTRL	PWM_PMFCTL	PWM_PMFCTL	0xF0C1	
Fault Status/Acknowledge Regis.	FLTACK	PMFSA	PWM_FLTACK	PWM_PMFSA	PWM_PMFSA	0xF0C2	
Output Control Register	OUT	PMOUT	PWM_OUT	PWM_PMOUT	PWM_PMOUT	0xF0C3	
Counter Register	CNTR	PMCNT	PWM_CNTR	PWM_PMCNT	PWM_PMCNT	0xF0C4	
Counter Modulo Register	CMOD	MCM	PWM_CMOD	PWM_MCM	PWM_MCM	0xF0C5	
Value 0-5 Registers	VAL0-5	PMVAL0-5	PWM_VAL0-5	PWM_PMVAL0-5	PWM_PMVAL0-5	0xF0C6	0xF0CB
Deadtime 0-1 Registers	DTIM0-1	PMDEADTM0-1	PWM_DTIM0-1	PWM_PMDEADTM0-1	PWM_PMDEADTM0-1	0xF0CC	0xF0CD
Disable Mapping 1-2 Registers	DMAP1-2	PMDISMAP1-2	PWM_DMAP1-2	PWM_PMDISMAP1-2	PWM_PMDISMAP1-2	0xF0CE	0xF0CF
Configure Register	CNFG	PMCFG	PWM_CNFG	PWM_PMCFG	PWM_PMCFG	0xF0D0	
Channel Control Register	CCTRL	PMCCR	PWM_CCTRL	PWM_PMCCR	PWM_PMCCR	0xF0D1	
Port Register	PORT	PMPORT	PWM_PORT	PWM_PMPORT	PWM_PMPORT	0xF0D2	
Internal Correction Control Register	ICCTRL	PMICCR	PWM_ICCTRL	PWM_PMICCR	PWM_PMICCR	0xF0D3	
Source Control Register	SCTRL	PMSRC	PWM_SCTRL	PWM_PMSRC	PWM_PMSRC	0xF0D4	
Synchronization Window Register	SYNC		PWM_SYNC	PWM_SYNC	PWM_SYNC	0xF0D5	
Fault Filter 0-3 Register	FFILT0-3		PWM_FFILT0-3	PWM_FFILT0-3	PWM_FFILT0-3	0xF0D6	0xF0D9
Multi-Scalable Controller Area Network (MSCAN) Module							
Control 0 Register	CTRL0		CAN_CTRL0		CANCTRL0	0XF800	
Control 1 Register	CTRL1		CAN_CTRL1		CANCTRL1	0XF801	
Bus Timing 0 Register	BTR0		CAN_BTR0		CANBTR0	0XF802	
Bus Timing 1 Register	BTR1		CAN_BTR1		CANBTR1	0XF803	
Receive Flag Register	RFLG		CAN_RFLG		CANRFLG	0XF804	
Receiver Interrupt Enable Register	RIER		CAN_RIER		CANRIER	0XF805	
Transmitter Flag Register	TFLG		CAN_TFLG		CANTFLG	0XF806	
Transmitter Interrupt Enable Register.	TIER		CAN_TIER		CANTIER	0XF807	
Transmitter Msg Abort Request Register	TARQ		CAN_TARQ		CANTARQ	0XF808	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Transmitter Message Abort Acknowledge Register	TAAK		CAN_TAAK		CANTAAK	0XF809	
Transmitter FIFO Selection Register	TBSEL		CAN_TBSEL		CANTBSEL	0XF80A	
Identifier Acceptance Control Register	IDAC		CAN_IDAC		CANIDAC	0XF80B	
Miscellaneous Register	MISC		CAN_MISC		CANMISC	0XF80D	
Receive Error Register	RXERR		CAN_RXERR		CANRXERR	0XF80E	
Transmit Error Register	TXERR		CAN_TXERR		CANTXERR	0XF80F	
Identifier Acceptance 0-3 Registers	IDAR0-3		CAN_IDAR0-3		CANIDAR0-3	0xF810	0xF813
Identifier Mask 0-3 Registers	IDMR0-3		CAN_IDMR0-3		CANIDMR0-3	0xF814	0xF817
Identifier Acceptance 4-7 Register	IDAR4-7		CAN_IDAR4-7		CANIDAR4-7	0xF818	0xF81B
Identifier Mask 4-7 Registers	IDMR4-7		CAN_IDMR4-7		CANIDMR4-7	0xF81C	0xF81F
Foreground Receive FIFO Register	RXFG		CAN_RXFG		CANRXFG	0xF82F	0xF820
Foreground Transmit FIFO Register	TXFG		CAN_TXFG		CANTXFG	0xF830	0xF83F
Power Supervisor (PS) Module							
Control Register	CTRL	LVICONTROL	PS_CTRL	LVICONTROL	LVICTRL	0xF140	
Status Register	STAT	LVISTATUS	PS_STAT	LVISTATUS	LVISR	0xF141	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Queued Serial Communications Interface (QSCI) Module							
					n=0, 1		
Baud Rate Register	RATE		QSCI_RATE		QSCI_SCIBR	0xF2***n***0	
Control 1 Register	CTRL1		QSCI_CTRL1		QSCI_SCICR	0xF2***n***1	
Control 2 Register	CTRL2		QSCI_CTRL2		QSCI_SCICR2	0xF2***n***2	
Status Register	STAT		QSCI_STAT		QSCI_SCISR	0xF2***n***3	
Data Register	DATA		QSCI_DATA		QSCI_SCIDR	0xF2***n***4	
Queued Serial Peripheral Interface (QSPI) Module							
Status and Control Register	SCTRL		QSPI_SCTRL		QSPI_SPSCR	0xF2***n***0	
Data Size and Control Register	DSCTRL		QSPI_DSCTRL		QSPI_SPDSR	0xF2***n***1	
Data Receive Register	DRCV		QSPI_DRCV		QSPI_SPDRR	0xF2***n***2	
Data Transmit Register	DXMIT		QSPI_DXMIT		QSPI_SPDTR	0xF2***n***3	
FIFO Control Register	FIFO		QSPI_FIFO		QSPI_SPFIFO	0xF2***n***4	
Wait Register	WAIT		QSPI_WAIT		QSPI_SPWAIT	0xF2***n***5	
Quad-Timer (TMR) Module							
					n=0, 1, 2, 3		
Compare 1 Register	COMP1	TMRCMP1	TMR***n***_COMP1	TMR***n***_CMP1	TMR***n***_CMP1	0xF0***n***0	
Compare 2 Register	COMP2	TMRCMP2	TMR***n***_COMP2	TMR***n***_CMP2	TMR***n***_CMP2	0xF0***n***1	
Capture Register	CAPT	TMRCAP	TMR***n***_CAPT	TMR***n***_CAP	TMR***n***_CAP	0xF0***n***2	
Load Register	LOAD	TMRLOAD	TMR***n***_LOAD	TMR***n***_LOAD	TMR***n***_LOAD	0xF0***n***3	
Hold Register	HOLD	TMRHOLD	TMR***n***_HOLD	TMR***n***_HOLD	TMR***n***_HOLD	0xF0***n***4	
Counter Register	CNTR	TMRCNTR	TMR***n***_CNTR	TMR***n***_CNTR	TMR***n***_CNTR	0xF0***n***5	
Control Register	CTRL	TMRCTRL	TMR***n***_CTRL	TMR***n***_CTRL	TMR***n***_CTRL	0xF0***n***6	
Status and Control Register	SCTRL	TMRSCR	TMR***n***_SCTRL	TMR***n***_SCR	TMR***n***_SCR	0xF0***n***7	
Comparator Load 1 Register	CMPLD1	TMRCMPLD1	TMR***n***_CMPLD1	TMR***n***_CMPLD1	TMR***n***_CMPLD1	0xF0***n***8	
Comparator Load 2 Register	CMPLD2	TMRCMPLD2	TMR***n***_CMPLD2	TMR***n***_CMPLD2	TMR***n***_CMPLD2	0xF0***n***9	
Comparator Status/Control Register	CSCTRL	TMRCOMSCR	TMR***n***_CSCTRL	TMR***n***_COMSCR	TMR***n***_COMSCR	0xF0***n***A	
Input Filter Register	FILT		TMR***n***_FILT	TMR***n***_FILT	TMR***n***_FILT	0xF0***n***B	
Enable Register	ENBL		TMR***n***_ENBL	TMR***n***_ENBL	TMR***n***_ENBL	0xF0***n****F*	
Voltage Regulator (VREG) Module							
See SIM section							

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Programmable Interval Timer (PIT) Module							
					n=0, 1, 2		
Control Register	CTRL		PIT***n***_CTRL	PITCTRL0-2	PIT***n***_CTRL	0xF1***n***0	
Modulo Register	MOD		PIT***n***_MOD	PITMOD0-2	PIT***n***_MOD	0xF1***n***1	
Counter Register	CNTR		PIT***n***_CNTR	PITCNTR0-2	PIT***n***_CNTR	0xF1***n***2	
					n=0, 1		
Control Register	CTRL		DAC***n***_CTRL	DACCTRL0-2	DAC***n***_CTRL	0xF1***n***0	
Data Register	DATA		DAC***n***_DATA	DACDATA0-2	DAC***n***_DATA	0xF1***n***1	
Step Register	STEP		DAC***n***_STEP	DACSTEP0-2	DAC***n***_STEP	0xF1***n***2	
Minimum Value Register	MINVAL		DAC***n***_MINVAL	DACMINVAL0-2	DAC***n***_MINVAL	0xF1***n***3	
Maximum Value Register	MAXVAL		DAC***n***_MAXVAL	DACMAXVAL0-2	DAC***n***_MAXVAL	0xF1***n***4	
Comparator (CMP) Module							
					A x=E ***B x***=F		
Control Register	CTRL		CMP_CTRL	CMP***x***_CTRL	CMP***x***_CTRL	0xF1***x***0	
Status Register	STAT		CMP_STAT	CMP***x***_STAT	CMP***x***_STAT	0xF1***x***1	
Filter Register	FILT		CMP_FILT	CMP***x***_FILT	CMP***x***_FILT	0xF1***x***2	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Interrupt Controller (ITCN) Module							
Interrupt Priority 0-4 Registers	N/A	N/A	ITCN_IPR0-4	ITCN_IPR0-4	INTC_IPR0-4	0XF060	0XF064
Vector Base Address Register	N/A	N/A	ITCN_VBA	ITCN_VBA	INTC_VBA	0XF065	
Fast Interrupt Match 0 Register	N/A	N/A	ITCN_FIM0	ITCN_FIM0	INTC_FIM0	0XF066	
Fast Interrupt Vector Address Low 0	N/A	N/A	ITCN_FIVAL0	ITCN_FIVAL0	INTC_FIVAL0	0XF067	
Fast Interrupt Vector Address High 0	N/A	N/A	ITCN_FIVAH0	ITCN_FIVAH0	INTC_FIVAH0	0XF068	
Fast Interrupt Match 1 Register	N/A	N/A	ITCN_FIM1	ITCN_FIM1	INTC_FIM1	0xF069	
Fast Interrupt Vector Address Low 1	N/A	N/A	ITCN_FIVAL1	ITCN_FIVAL1	INTC_FIVAL1	0xF06A	
Fast Interrupt Vector Address High 1	N/A	N/A	ITCN_FIVAH1	ITCN_FIVAH1	INTC_FIVAH1	0xF06B	
Interrupt Pending 0 Register	N/A	N/A	ITCN_IRQP0	ITCN_IRQP0	INTC_IRQP0	0xF06C	
Interrupt Pending 1 Register	N/A	N/A	ITCN_IRQP1	ITCN_IRQP1	INTC_IRQP1	0xF06D	
Interrupt Pending 2 Register	N/A	N/A	ITCN_IRQP2	ITCN_IRQP2	INTC_IRQP2	0xF06E	
System Integration Module (SIM)							
Control Register	N/A	N/A	SIM_CTRL	SIM_CONTROL	SIM_CONTROL	0xF100	
Reset Status Register	N/A	N/A	SIM_RSTAT	SIM_RSTSTS	SIM_RSTSTS	0xF101	
Software Control 0-3 Registers	N/A	N/A	SIM_SWC0-3	SIM_SCR0-3	SIM_SCR0-3	0xF102	0xF105
Most Significant Half JTAG ID	N/A	N/A	SIM_MSHID	SIM_MSH_ID	SIM_MSH_ID	0xF106	
Least Significant Half JTAG ID	N/A	N/A	SIM_LSHID	SIM_LSH_ID	SIM_LSH_ID	0xF107	
Power Control Register	N/A	N/A	SIM_PWR	SIM_POWER		0xF108	
Clock Out Select Register	N/A	N/A	SIM_CLKOUT	SIM_CLKOSR	SIM_CLKOSR	0xF10A	
Peripheral Clock Rate Register	N/A	N/A	SIM_PCR	SIM_PCR	SIM_PCR	0xF10B	
Peripheral Clock Enable 0-1 Register	N/A	N/A	SIM_PCE0-1	SIM_PCE0-1	SIM_PCE0-1	0xF10C	0xF10D
Peripheral Stop Disable 0-1 Register	N/A	N/A	SIM_SD0-1	SIM_SD0-1	SIM_SD0-1	0xF10E	0xF10F

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
I/O Short Address Location High Register	N/A	N/A	SIM_ISALH	SIM_ISALH	SIM_ISALH	0xF110	
I/O Short Address Location Low Register	N/A	N/A	SIM_ISALL	SIM_ISALL	SIM_ISALL	0xF111	
Protection Register	N/A	N/A	SIM_PROT	SIM_PROT	SIM_PROT	0xF112	
GPIOA Peripheral Select 0 Register	N/A	N/A	SIM_GPISA0	SIM_GPISA0	SIM_GPISA0	0xF113	
GPIOA Peripheral Select 0 Register	N/A	N/A	SIM_GPSA1	SIM_GPSA1	SIM_GPSA1	0xF114	
GPIOB Peripheral Select 0 Register	N/A	N/A	SIM_GPSB0	SIM_GPSB0	SIM_GPSB0	0xF115	
GPIOB Peripheral Select 1 Register	N/A	N/A	SIM_GPSB1	SIM_GPSB1	SIM_GPSB1	0xF116	
GPIO Perip. Select Register for GPIO C & D	N/A	N/A	SIM_GPSCD	SIM_GPSCD	SIM_GPSCD	0xF117	
Internal Peripheral. Select Register for PWM	N/A	N/A	SIM_ISPWM	SIM_ISPWM	SIM_ISPWM	0xF118	
Internal Peripheral Select Register for DAC	N/A	N/A	SIM_IPSDAC	SIM_IPSDAC	SIM_IPSDAC	0xF119	
Internal Peripheral Select Register for TMRA	N/A	N/A	SIM_IPSTMRA	SIM_IPSTMRA	SIM_IPSTMRA	0xF11A	

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